TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE

(From JEDEC Board Ballot JC-15.1-04-268A formulated under the cognizance of the JC15.1 Committee on thermal characterization.)

Contents

1 Scope

This guideline specifies the definition and construction of a two-resistor compact thermal model (CTM) from the JEDEC junction-to-case and junction-to-board thermal metrics. The guidance provided in this document only applies to thermal metrics defined in JEDEC standards JESD51-8 and JESD51-12.

The scope of this document is limited to single-die packages that can be effectively represented by a single junction temperature.

2 Normative references

1. JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*, Dec. 1995.
2. JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*, Dec. 1995.
3. JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,* Aug. 1996.
4. JESD51-5, *Extension of Thermal Test Board Standards For Packages With Direct Thermal Attachment Mechanisms*, Feb. 1996.
5. JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*, March 1999.
6. JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, Feb. 1999.
7. JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*, Oct. 1999.
8. JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements,* July 2000.
9. JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements,* July 2000.
10. JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurement*, June 2001.
11. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, May 2005.
12. JESD15, *Thermal Modeling Overview* [1)].
13. JESD15-1, *Compact Thermal Modeling Overview* [1)].

[1)] To be published.

14. JESD15-2, *Terms and Definitions for Modeling Standards* [1)].

15. JESD15-4, *DELPHI Compact Thermal Model Guideline* [1)].

3 Definition of the two-resistor compact thermal model

3.1 Overview

Excluding the single-parameter metrics such as θ_{JA}, the two-resistor compact model is the simplest and most intuitive of compact thermal models and occupies an important place in the spectrum of compact modeling methodologies as stated in JESD15-1. Although other compact model approaches (see JESD15-4) do exist that have a demonstrated higher accuracy, the simplicity and intuitiveness of a two-resistor model are attractive features. However, accuracy of such models remains a concern. Users should exercise care in using two-resistor model data for predicting package temperatures.

The two-resistor model definition describes the thermal behavior of the chip package itself and its interconnection to the environment. The environmental conditions themselves are not a part of the model and must be specified by the user in terms of boundary conditions for the relevant application.

3.2 General Criteria for compact thermal models

A compact thermal model should fulfil the following criteria.

- It should be of limited complexity. In today's technology, this equates to tens of nodes. It is conceivable that this number could increase over time with improvements in computer calculating power and the sophistication of CTM techniques.
- It should satisfy appropriate levels of boundary condition independence (BCI). BCI is a property of a CTM whereby it accurately calculates a chip temperature in a variety of application environments, which, in essence, impose different boundary conditions on the component. It is a goal of the CTM standardization effort that CTMs should demonstrate a high level of BCI.
- It should be vendor and software neutral.
- A CTM generation technique should be adaptable to standard conduction codes for performing a package-level thermal analysis.
- The CTM should be capable of insertion into standard numerical codes for system-level analysis.
- It should be fully documented and non-proprietary.

3.3 The two-resistor methodology

The following are the key features of the two-resistor methodology.

- The compact model is generated from JEDEC standard tests for junction-to-case resistance (θ_{JCtop}) and junction-to-board resistance (θ_{JB}). If measured values are not available, simulated values can be used (see 3.4).
- The starting point for the process is the availability of a part sample.
- The resulting compact model contains artifacts from the test environments.

- An error estimate is not available during the model generation process.
- Like the other compact model approaches, the two-resistor compact model approach serves to mask data about the package that the supplier may regard as proprietary.

3.4 Network model definition

The JEDEC two-resistor model consists of three nodes as depicted in Figure 1. These are connected together by two thermal resistors which are the measured values of the junction-to-board (θ_{JB}, JEDEC Standard JESD51-8) and junction-to-case (θ_{JCtop}, discussed in JEDEC Guideline JESD51-12) thermal resistances described above.

For packages which are designed to inject heat directly on to the ground plane of the board, such as exposed pad packages, the user may consider replacing θ_{JB} by $\theta_{JCbottom}$.

If measured values are not available, simulated values of the junction-to-board and junction-to-case resistances can be used in constructing the two-resistor model, provided that the simulation approach has been validated to yield results equivalent to the measured results. Any simulated values must be indicated as such.

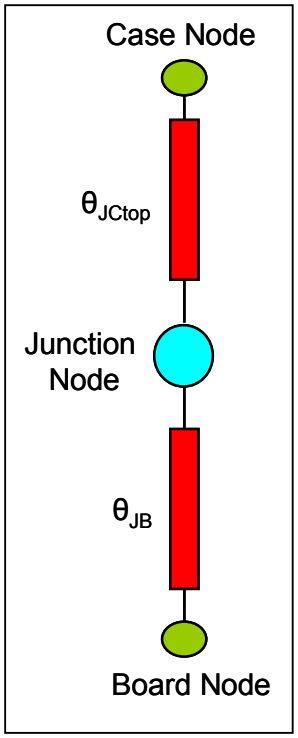

Figure 1 — Two-resistor model network

The heating power, P_H, is applied at the junction node.

The board node is considered to be in direct thermal contact with the local environment immediately below the footprint of the package; normally the printed circuit board (PCB).

The case node is considered to be in direct thermal contact with the local environment immediately above the top of the package (normally air, or a thermal interface material used in conjunction with a heat sink).

Thus there are only two paths for the heat to leave the junction node and flow into the environment - through the case node and through the board node. The model does not account for heat flow through the sides of the package.

4 Determination of the metrics

4.1 Junction-to-board thermal resistance (θ_{JB})

This parameter is measured in a ring cold plate fixture (see JESD51-8). This test fixture is designed to ensure that all the heat generated in the package is conducted to the cold plate via the board.

The metric is defined as:

$$\theta_{JB} = (T_J - T_B) / P_H$$

where θ_{JB} = thermal resistance from junction-to-board (ºC/W)

T_J = junction temperature when the device has achieved steady-state after application of P_H (ºC)

T_B = board temperature, measured at the mid point of the longest side of the package no more than 1mm from the edge of the package body (ºC)

P_H = heating power which produced the change in junction temperature (W)

It is important to note that the θ_{JB} metric includes a contribution from the thermal resistance of the test board. Therefore, the thermal conductivity of the board affects the measurement results. The JESD51-8 standard requires that the metric be measured on a 2s2p board defined in JESD51-7, 9, 10, or 11. Measurement of the board temperature very close to the edge of the package body is also intended to minimize the contribution from the board.

Further details are available in JESD51-8.

4.2 Junction-to-case thermal resistance (θ_{JCtop})

The metric is measured in a top cold plate fixture and is defined as:

$$\theta_{JCtop} = (T_J - T_{Ctop}) / P_H$$

where θ_{JCtop} = thermal resistance from junction-to-case (ºC/W)

T_J = junction temperature when the device has achieved steady-state after application of P_H (ºC)

T_{Ctop} = case temperature, measured at center of the package top surface (ºC)

P_H = heating power in the junction that causes the difference between the junction temperature T_J and the case temperature T_{Ctop}; this is equal to the power passing through the cold plate (W)

The method employed to measure θ_{JCtop} must be reported[2)]. The JESD51-12 standard provides a detailed discussion of the θ_{JCtop} metric.

5 Alternative metrics

The two-resistor model guideline requires that the model be constructed from θ_{JB} and θ_{JCtop} as explained in this document. However, the question arises as to whether alternative metrics can be substituted in case either of these metrics are not available.

Where a θ_{JB} value is unavailable, the value for ψ_{JB} measured on a 2s2p board in accordance with θ_{JMA} specification, JESD51-6, at zero forced air velocity can be used as an alternative, recognizing that this changes the value predicted by the resulting model. If ψ_{JB} is indeed used in place of θ_{JB}, then this should be clearly stated when the two-resistor model is published or disseminated.

Note that it is not possible to substitute ψ_{JT} for θ_{JCtop} in the creation of the two-resistor model as ψ_{JT} is a thermal characterization parameter. Thermal characterization parameters are not thermal resistances. This is because when the parameter is measured, the component power is flowing out of the component through multiple paths. ψ_{JT} is often significantly lower than θ_{JCtop}.

For packages which are designed to inject heat directly on to the ground plane of the board, such as exposed pad packages, the user may consider replacing θ_{JB} by $\theta_{JCbottom}$.

6 Application considerations

6.1 Overview

The two-resistor model can be used at various stages during the design process. During the initial stage of the design it can be used in back-of-the-envelope calculations to assess the possible bounds of the package behavior. As the design progresses, the model can be used in more detailed simulation tools that either directly support such a model, or provide the basic building blocks from which the model can be built. The simulation tool could belong to either of the following classes:

- thermal network calculator,
- three-dimensional simulation tool.

It is important to keep in mind that the two-resistor model does not eliminate the need for understanding the application in which the package is to be used. In other words, it is the user's responsibility to take into account the environment surrounding the package. The

[2)] JEDEC Standard JESD51-13, which will define the method for measuring θ_{JCtop}, is currently in preparation.

environmental conditions for the relevant application must be applied at the package top and bottom surfaces (i.e., case and board nodes) as boundary conditions.

6.2 Network calculator/spreadsheet-based tools

A network resistance calculation involves the representation of a thermal system in the form of a resistance network, similar to an electrical resistor network. Thus the individual components in the system must be represented by thermal resistances, and the paths between them defined. Heat generating objects must also be associated with thermal sources.

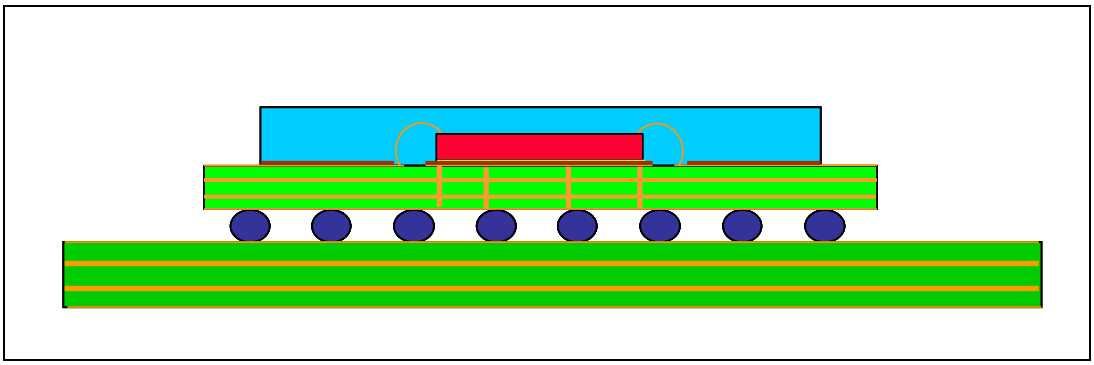

Figure 2 — Package on PCB

For a single package placed on a PCB in an airflow environment (see Figure 2), the equivalent thermal resistance network diagram of the package and environment could be drawn (see Figure 3) with the package represented by a two-resistor model.

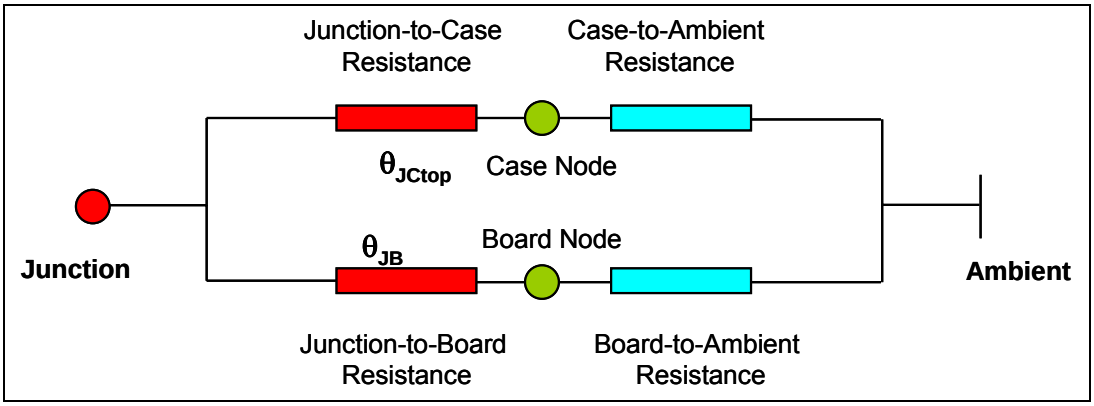

Figure 3 — Equivalent thermal resistance diagram of two-resistor model on PCB

In many cases, the operating board temperature can either be guessed, or else supplied as a constraint. In this case, it is not necessary to know the board-to-ambient resistance. The network can then be drawn as shown in Figure 4.

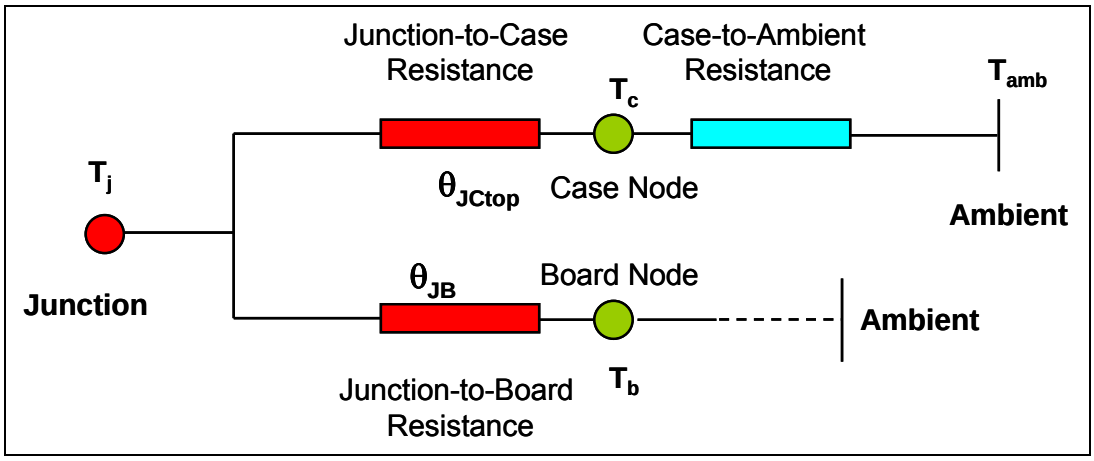

Figure 4 — Thermal resistance diagram of system with known board temperature

If the two-resistor model is known, then the unknowns in the resistance network are the case-to-ambient resistance and the board-to-ambient resistance.

Estimating the case-to-ambient resistance depends on the environmental conditions on the package case. If the package is bare (without a heat sink), then the heat transfer coefficient on its surface must be determined or guessed in some manner. Rather than using flat-plate correlations it is preferable to use heat transfer coefficients from test data or assume a value based on the heat transfer regime. Approximate ranges for heat transfer coefficients (h.t.c.'s) for different cooling regimes in typical electronics cooling situations are shown in Table 1.

Table 1 — Typical cooling regimes in electronics

Cooling Regime	Approximate Heat Transfer Coefficient Range (W/m^2K)
Natural Convection, Air	2 - 30
Forced Convection, Air	15 - 300
Forced Convection, Water	200 – 10,000
Pool Boiling, Water	3000 – 50,000

If a heat sink is present, however, the thermal resistance value of the heat sink can be directly used. This case-to-ambient thermal resistance is made of two parts – a case-to-sink resistance, normally the resistance of the attachment material that binds the heat sink to the package, and sink-to-ambient resistance, which will normally be supplied by the manufacturer of the heat sink.

6.3 Three-dimensional modeling and simulation tools

6.3.1 Overview

This class of software tools solves the constitutive equations governing heat transfer in a 3D domain using numerical discretization schemes. Thus, solving for the junction temperature does not involve the solution of a network-type equation for the environment, but rather a set of simultaneous differential equations.

In most practical applications, the numerical simulation also involves discretizing the solution domain, which is achieved by a process known as gridding (or meshing). The accuracy of the solution is affected by the grid density. The grid density is sufficiently high when any additional increase in grid has only a small effect on the results. To account for radiation heat transfer all external surfaces that participate in radiation exchange to a significant degree need to be identified and appropriate emissivities assigned.

Broadly speaking, three-dimensional modeling tools fall into two categories:

- conduction simulation tools
- computational fluid dynamics (CFD) simulation tools

6.3.2 Conduction-focused tools

Conduction-focused tools solve the governing equations for conduction heat transfer (and often radiation) within the solid portions of the system. The effects of the airflow are not solved for directly, but are instead represented at the solid-air interface in the form of equivalent heat transfer coefficients. In the case of a two-resistor model, appropriate heat transfer coefficients need to be applied at surfaces that directly interface with the fluid environment. The heat transfer coefficients are attached to the compact model (Figure 5) at those surface nodes exposed to the fluid only. The surfaces in contact with the PCB and/or a heat sink are handled within the conduction heat transfer calculation.

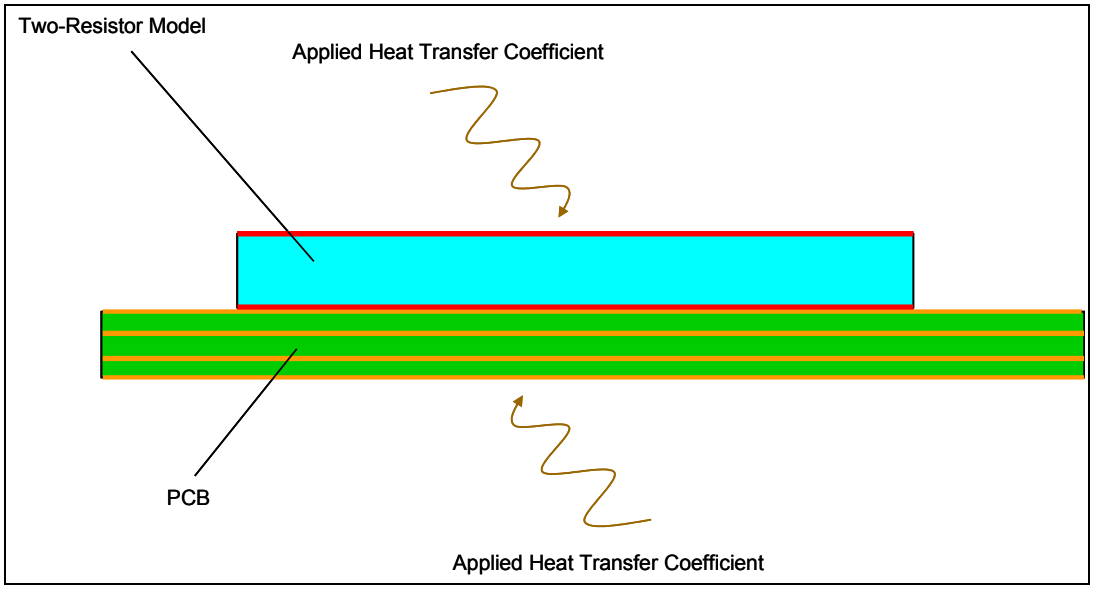

Figure 5 — Two-resistor model in conduction-only simulation environment

6.3.3 Computational fluid dynamics (CFD) tools

CFD tools solve both the solid and air portions of the system directly. This is achieved by solving the Navier-Stokes equations, which govern fluid flow and heat transfer, on the air side. In the solid portions, equations governing conduction heat transfer are solved. Nearly all CFD tools available also solve for radiation heat transfer. Because CFD tools explicitly model the airflow (convection) in addition to doing so for conduction and radiation modes of heat transfer (see Figure 6), it is not necessary for heat transfer coefficients to be applied to the model.

In a CFD tool, attention should be paid to the representation of the external physical geometry of the package to ensure the correct interaction between the package and surrounding air flow. In other words, the two-resistor model should produce the same effect on the outer flow as the actual package. This means that the compact model must ideally result in the same flow resistance (i.e., pressure drop) as the actual package. It must also provide a similar thermal interaction with this environment. Thus, from a top view, the size of the model should match the outline of the package body. The height of the model should also match the overall height of the package when mounted.

Surface emissivity is applied to the exposed surfaces, usually as a surface attachment, in order to account for radiation heat transfer.

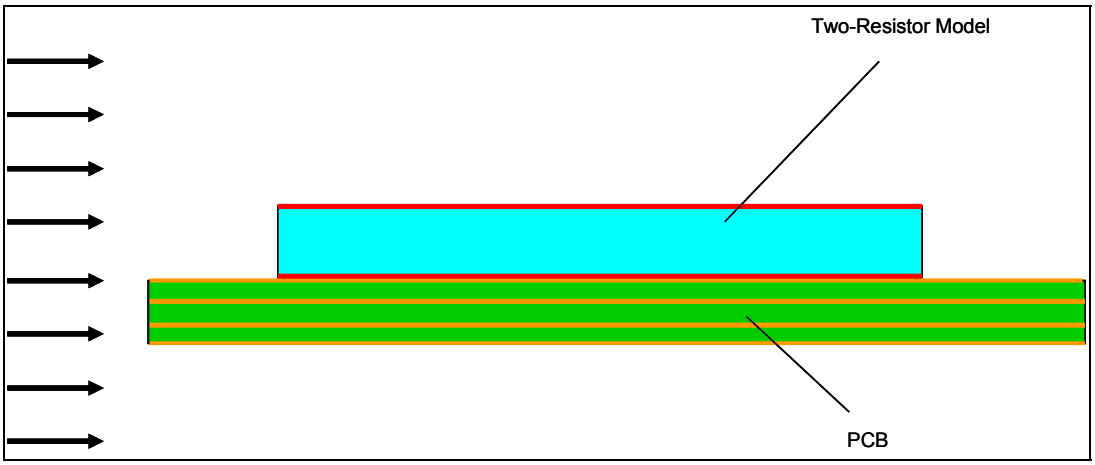

Figure 6 — Two-resistor model in CFD simulation environment

6.3.4 Representing a two-resistor model in 3D space

There are several viable approaches to representing the two-resistor model in 3D space, which is required for both conduction-focused and CFD tools. Essentially the problem involves representing the resistor network in Figure 1 in three-dimensional space. Some constraints are common to all representations, such as:

- The case and board nodes of the two-resistor model are, by definition, isothermal, with case node temperature at T_C and the board node temperature at T_B.

- The two-resistor model must closely approximate the effect on the environment of the actual package.
- The surfaces of attachment of the model to the PCB and/or a heat sink should be as identical as feasible to the actual package.
- The two-resistor model is not allowed to "leak" heat from its sides. The only surfaces through which heat can be exchanged with the environment are the top and bottom surfaces, i.e., the case and the board nodes.

It is the end-user's responsibility to apply the environmental conditions for the application environment at the surface nodes of the compact model. This can be done either by modelling the environment in detail or by prescribing effective boundary conditions in terms of heat transfer coefficients. This will be constrained by the class of software tools available to the end-user. Some tools may allow a more precise description of the boundary conditions than others.

Some of the approaches that can be used to represent a two-resistor model in three-dimensional space are

- block-and-plate method,
- block-and-surface resistance method, and
- network object method.

6.3.4.1 Block-and-plate method

A classic configuration that can represent such a network is an isothermal "block", thermally insulated on its sides, and sandwiched between two "plates" (Figure 7). A block is a cuboid that is capable of conducting heat in all three directions within its body. A "plate" is defined here as a geometrically 2D object, i.e., it has no geometric thickness. It cannot conduct heat in the in-plane directions and is limited to heat transfer in the normal direction only. In this scheme, a block is used to represent a node, while a plate represents a resistance.

More specifically, the block represents the junction node, whereas the top plate and the bottom plate represent the junction-to-case and junction-to-board resistances respectively. The insulated sides ensure that there is no heat "leakage" out of the one-dimensional path of the network. It is also important that the block be isothermal, as a node is by definition, an isothermal entity. In practice this requires assigning a suitably high conductivity for the cuboid block such that the additional, unwanted conduction resistance introduced due to its presence is negligible. The block conductivity should be such that this unwanted resistance is at least two orders of magnitude lower than either junction-to-case or junction-to-board resistances.

The size of the block should be as close as possible to the size of the actual package. The plate representing the junction-to-board resistance contacts the PCB, with the contact area being equal to the bottom surface area of the block.

The thickness and conductivity of the plates can be set to any value as long as the resultant thermal resistance is equal to the value of θ_{JCtop} or θ_{JB}. The formula relating the plate thermal resistance to the plate thickness (t), plate surface area (A), and thermal conductivity of the plate material (k) is:

Thermal resistance (θ_{JCtop} or θ_{JB}) = t / kA

The heat in the compact model is introduced through a "heat source" object. A heat source is essentially an area or a volume (or sometimes a point) which introduces a heat flux uniformly across itself into the block. The heat source is placed within the body of the block. As far as representing the heat dissipation in a two-resistor model is concerned, a volume heat source is preferable to an area heat source. A point heat source should not be used.

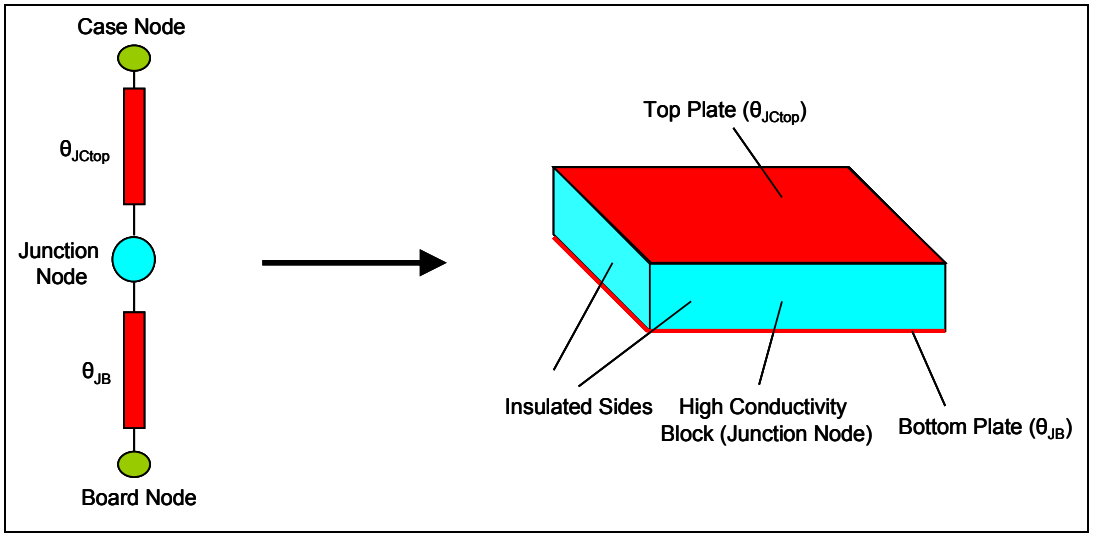

Figure 7 — Two-resistor model represented in 3D space using a block-and-plate approach

6.3.4.2 Block-and-surface resistance method

The block-and-surface resistance approach (Figure 8) is similar to the block-and-plate approach except for the representation of the resistors. Instead of using Plates to represent the junction-to-case and junction-to-board resistances, a surface property is assigned to the appropriate surfaces of the block. Such a surface property builds a thermal resistance automatically on the assigned surface, thus making it unnecessary to use an explicit object for this purpose.

The representation of the contact area and heat dissipation in this method is identical to that in the block-and-plate method described above.

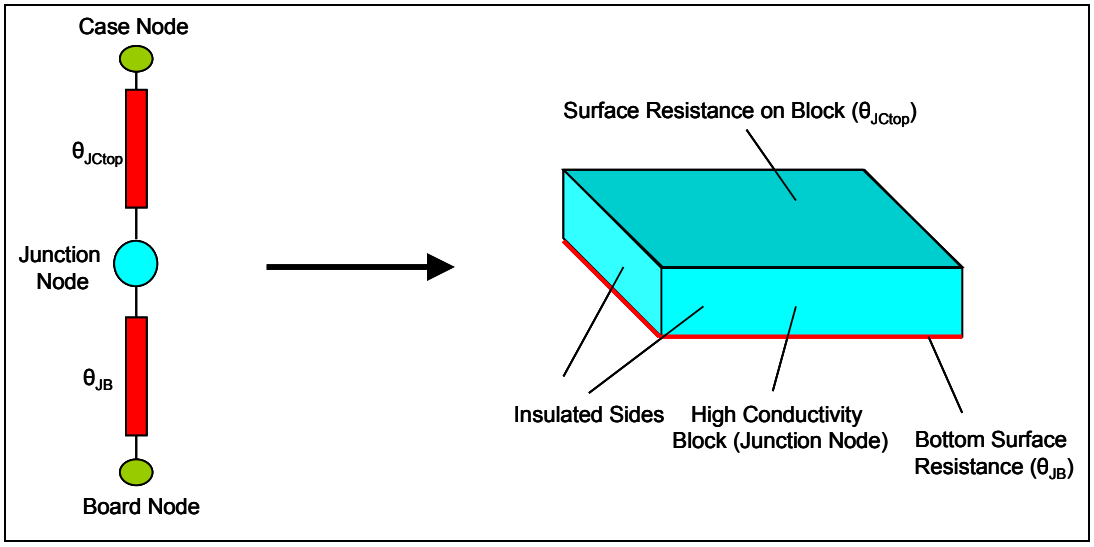

Figure 8 — Two-resistor model represented using a block-and-surface resistance approach

6.3.4.3 Network object method

The third approach utilizes what may be called a "network object" (Figure 9) to represent the two-resistor model. Such an object has a three-dimensional external shape in order to model the obstruction caused by the package to the outer flow and the heat transfer to the environment.

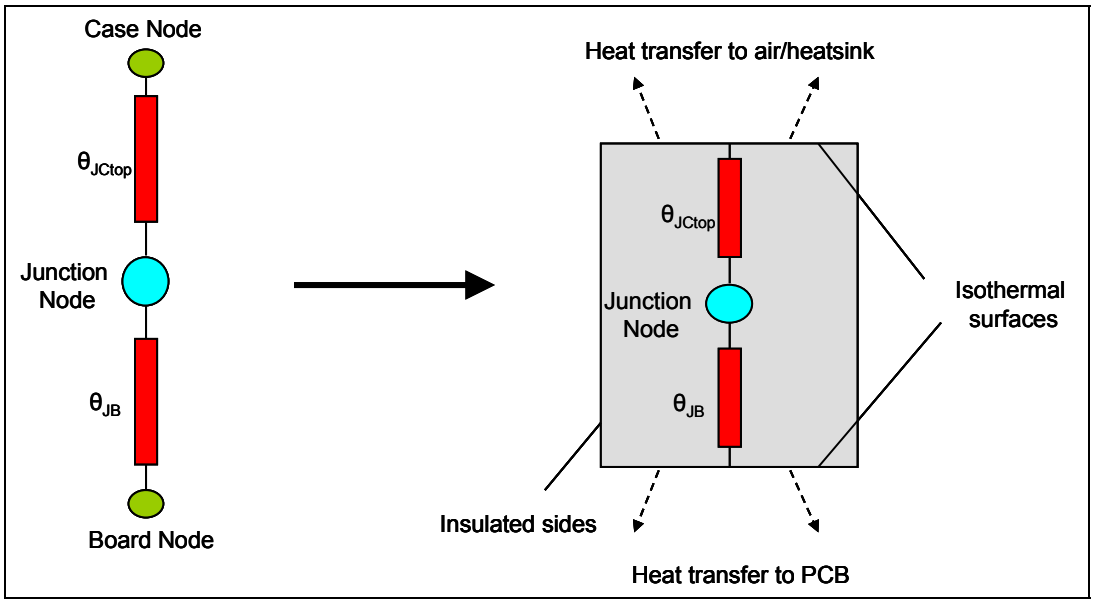

Figure 9 — Two-resistor model as a three-dimensional network object

However, instead of reproducing the resistor links as conducting solids, a resistor network solver is directly linked to the inputs from the surface nodes of this blockage.

6.4 Accuracy bounds of a two-resistor model

It should be noted that the magnitude of the error in junction temperature prediction in a specific situation in which a two-resistor model is used cannot be known *a priori*, as the error bounds for this model cannot be obtained from its generation process. They may be derived by comparison of junction temperature predictions of two-resistor models compared with actual tests or validated detailed models[3)]. The model may under-predict or over-predict the true value. In general, the model's predictive accuracy is expected to be lower as the disparity between the specific application environment and the JEDEC test environments increases.

It should also be noted that the two-resistor model contains an artifact of the environment used for generation for area array packages. This is because θ_{JB} test requires that the board temperature be measured on the top trace of the PCB, within 1 mm of the package edge. The corresponding measurement for leaded packages is on the lead foot, thus eliminating any environment artifact in such cases. Thus a part of the board resistance is included in the measured value of θ_{JB}. This board contribution may or may not be small.

It is difficult to derive an absolute theoretical bound for the predictive error of a two-resistor compact model. However, several studies (see Bibliography) have shown typical errors for junction temperature rise over ambient for two-resistor models as compared to experimentally validated detailed models to be in the neighborhood of 30% or less. This figure should merely be used as a guide– it is by no means a definitive error bound. Users should exercise care in using two-resistor model data for predicting the absolute values of package temperatures.

7 Methodology for constructing and using two-resistor model

7.1 Two-resistor model construction and usage

A summary of the steps necessary to construct and implement a two-resistor compact model is presented below.

1) Conduct the θ_{JB} and θ_{JCtop} tests using the prescribed test hardware. Measure and extract the metrics θ_{JB} and θ_{JCtop}. If θ_{JB} is not available, ψ_{JB} can be used under the caveats stated in 5. See also document JESD51-12.
2) Report the metric values, package power, and external geometry of the package in question. External geometry refers to the height of the package, the top exposed area, and area in contact with the PCB.
3) Report the emissivity of the exposed surfaces of the package.
4) If a three-dimensional representation of the model is to be used:
    - Generate a solid model that has a size and profile as close as possible to the actual package.
    - Use the available building blocks in the software environment to construct a two-resistor network such that the resistances are represented appropriately.
    - Ensure that the correct heat dissipation is introduced in this model.

[3)] A detailed model of a package is a numerical model that attempts to reproduce the physical construction of the package as exactly as feasible.

- Ensure that appropriate emissivities are assigned to all exposed surfaces.
- Ensure that the sides are insulated, so that heat is transferred only in the top and bottom directions from the model.

7.2 Example illustrating the use of a two-resistor model

Assume that the package in question is a plastic ball grid array (PBGA) package of 35 mm body size with a published θ_{JC} value of 5.4 ºC/W and a θ_{JB} value of 11.9 ºC/W. P_H is specified as 2 W. Consider a situation in which this package is to be placed on a PCB, with an expected forced airflow of 1 m/s. The goal is to estimate the junction temperature under these conditions.

Assume that the ambient air temperature is 30 ºC while the board temperature is estimated as 60 ºC. Computing the junction temperature requires solving the series and parallel resistance network in Figure 4.

For forced air at 1 m/s assume that the heat transfer coefficient on the exposed top surface of the package is 15 W/m^{2}K (see Table 1). To calculate the case-to-ambient resistance we use the equation:

$$R = \frac{1}{hA}, \text{ where}$$

R = thermal resistance

h = heat transfer coefficient

A = surface area on which the heat transfer coefficient acts

Assuming the mold cap of the package has a size of 32 mm x 32 mm, the case-to-ambient resistance, θ_{CA}, is calculated as 66.0 ºC/W.

The network model for the entire system can now be drawn (see Figure 10).

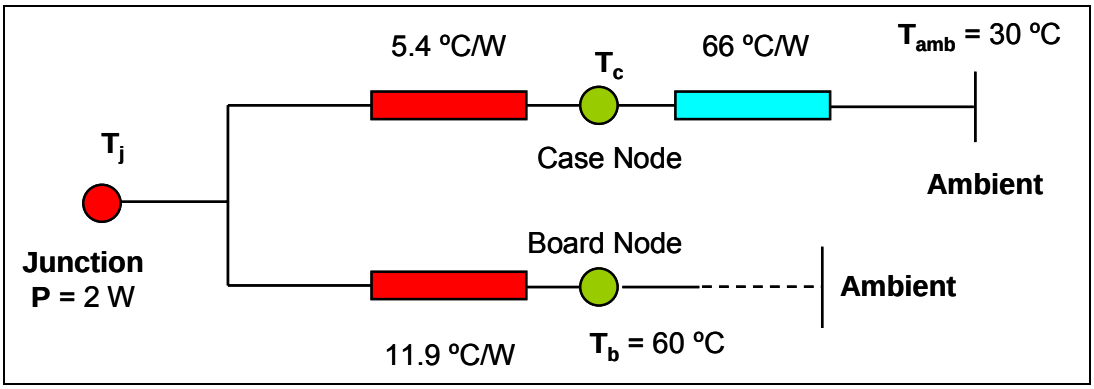

Figure 10 — Thermal resistance diagram for worked example

To solve this network, enforce the conservation of energy principle on both sides of the junction node. Thus, the net heat flowing out of the network is equal to the power generated at the junction. Summing the power flowing through each branch of the above network, and equating this to the total power applied at the junction, one gets:

$$\frac{T_j - 60}{11.9} + \frac{T_j - 30}{(66.0 + 5.4)} = 2$$

This is an algebraic equation in one unknown and can be solved to yield a T_j of 76.1 ºC.

Thus the junction temperature of this PBGA package on a PCB under a 1m/s forced air environment has been computed as being 76.1 ºC.

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