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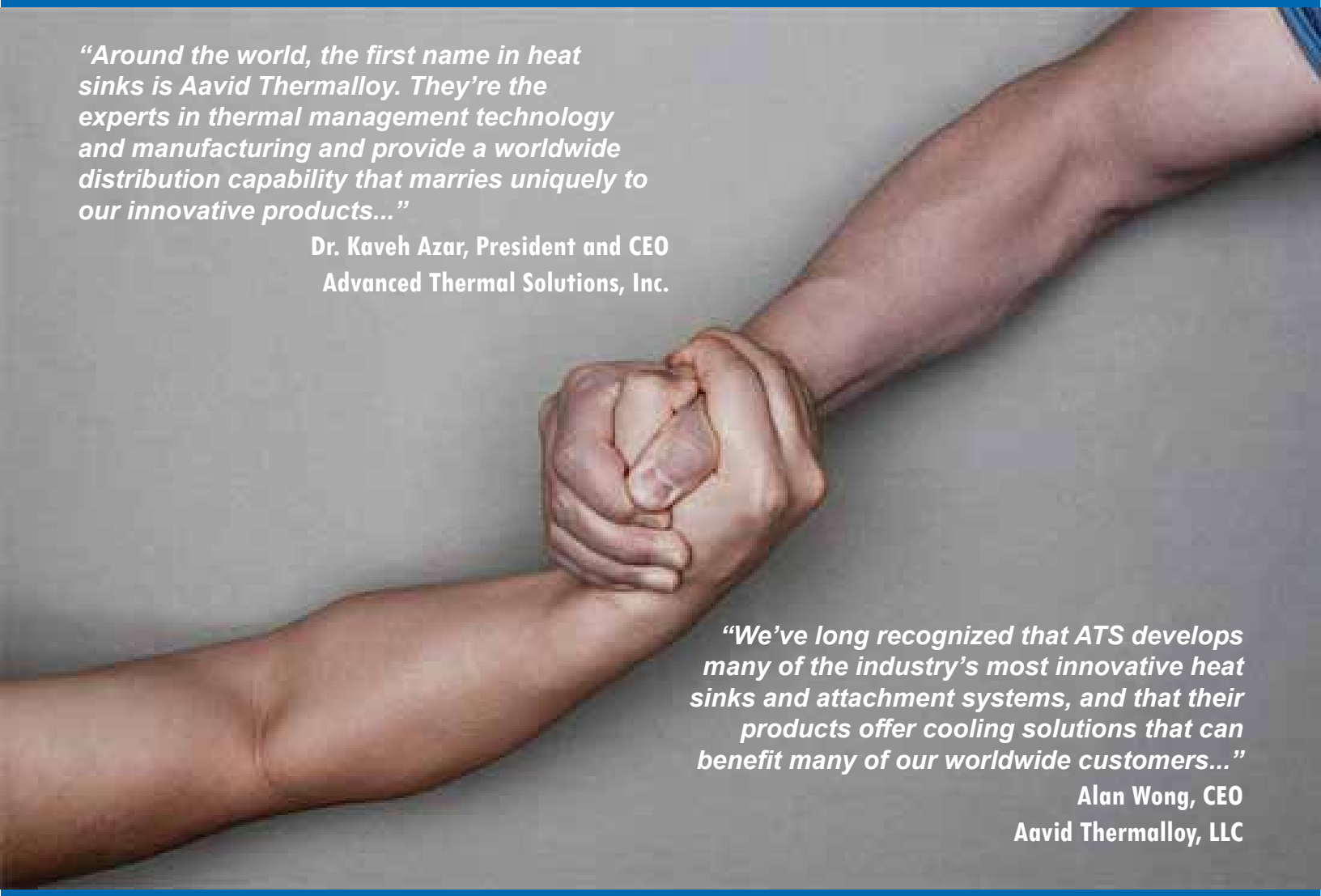
Features

TWO THERMAL MANAGEMENT POWERHOUSES JOIN FORCES



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ATCA Standards

For Thermo-Mechanical Considerations

In 2002, the PCI Industrial Computer Manufacturers Group (PICMG) released a set of specifications known as Advanced Telecommunications Computing Architecture (ATCA). Also known as AdvancedTCA, these are open specifications that were designed for "carrier grade" communications equipment [1]. The specifications were designed to accommodate the latest technologies and incorporate them into a modular approach. The specifications were open so that different manufacturers could make products that are compatible to each other, decreasing costs and simplifying operation.

Since the main point of the ATCA standards is interoperability, the actual list of standards is very long and detailed. The base specification, which doesn't even contain specifications for the Fabric (The method of data transmission), is a tome that would rival any college textbook. When working on projects that follow ATCA standards, the most important thing to remember is what types of things the standards dictate, and then it will be easy enough to look up the actual numbers.

ATCA is based around Front Board PCBs known as Blades. Blades plug into housings called Shelves, and can perform many different functions, such as routing data, providing server-based computing or housing mezzanine cards. In Figure 1 below, an example of a Blade is shown [2]. It would be correct to infer that Blades are often power-dense and must fit into a limited amount of space, judging by the use of expensive copper heat sinks and angled memory modules.

Figure 1- Example of an ATCA Blade [2]

Physically, the Front Board must be 280 D X 322.25 H (mm), which is approximately 11" X 13" [3]. The board may weigh up to 4 kg, and must fit into a slot that is 30.48 mm wide. Component keepout zones of 4.5 mm along the top and bottom edges of the board allow the board to slide into alignment rails in the housings in which they will reside. The board offset is dictated, of course, and leaves an allowance of 21.33 mm for maximum component height, as illustrated below in Figure 2. This leaves a 2.54 mm no-component zone between boards.

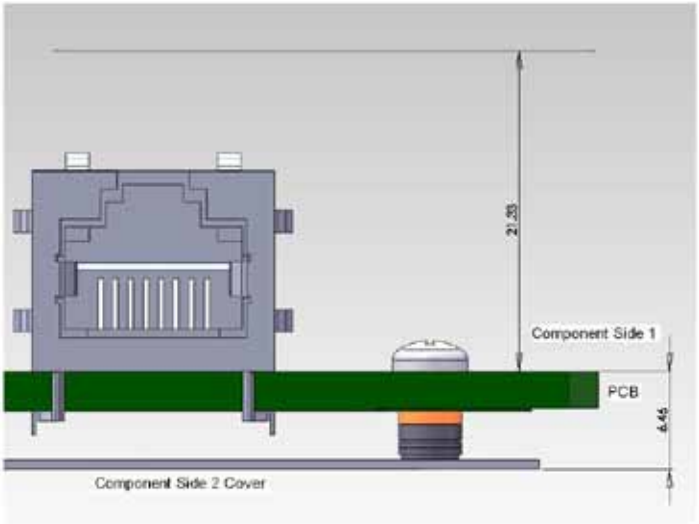

Figure 2- ATCA Front Board Component Height

Figure 2 also shows the required Component Side 2 cover, which must be metal to shield EMI and limit the spread of fire. After accounting for warpage of both the board and the cover, the component height on Side 2 is typically limited to less than 2 mm, and details are listed in the ATCA specification.

Other important requirements for the front board are a metal face plate with standardized LEDs, two handles and an EMI gasket. In addition to fixed dimensions for those parts, the handles must have switches on them to facilitate hot-swapping of boards. As the controlled discharge of static is important during board insertion, there are detailed specifications regarding ESD strips along the bottom edge of the board.

The ATCA specification also controls the connections that are made between boards and the Shelf, so that any ATCA compliant board will plug into any ATCA compliant chassis. The Zone 1 connector is bottommost on the board, and provides power for the board and communication with the shelf for shelf management functions (See Figure 3). The Zone 2 connector moves data between boards that may be inserted in the Shelf as well as to and from the outside network.

Figure 3- ATCA Front Board Connectors [4]

The Zone 3 connector is optional, and unlike Zone 1 and 2, neither the connector nor the pins are defined by the ATCA specification. The Zone 3 connector remains flexible in order to connect with a matching Rear Transition Module (RTM). The RTM usually holds I/O cables, so that the Front Board can be removed without disconnecting large amounts of wiring.

Figure 4- Example of a Rear Transition Module [2]

The RTM has specifications similar to the Front Board for height, width and board thickness, but it is only 70 mm deep. It is also required to have a face plate with handles and an EMI gasket, along with many other requirements that mirror the front panel.

The other important focus of the ATCA formula is the Shelf, the chassis that houses Blades and provides power and cooling to them. The Shelf comprises several elements including the Subrack, the Shelf Management Module (SHM), and the cooling system. The Subrack is the inner housing that the boards slide into. In Figure 5 below, the Zone 1 (blue) and Zone 2 connectors can be seen on the Backplane of the Subrack. As the Zone 1 and 2 connectors are standardized on all ATCA boards, they are also standardized on the Subrack.

Figure 5- Typical ATCA Chassis [5]

The Subrack is 8 rack units high and holds 14 ATCA boards. In the European standard ETSI rack, the Subrack holds 16 boards. The SHM, which can be seen just above the Subrack in Figure 5, determines if a blade can be powered up, and can also power down a blade if necessary. It also receives signals from on-Blade temperature sensors and can vary the fan speed to keep Blades cool. The cooling system of the Shelf is more loosely defined, and allows for forced or natural convection. Natural convection is usually not capable of meeting the cooling requirements of ATCA Blades, however, and is seldom seen. The typical airflow path of an ATCA Shelf is shown in Figure 6, but it is not a strict requirement. With the intake located at the bottom front and the exhaust at the top rear, the exhaust air stream blows into the maintenance aisle behind the Shelf. Note that the RTM must be cooled along with the Front Board.

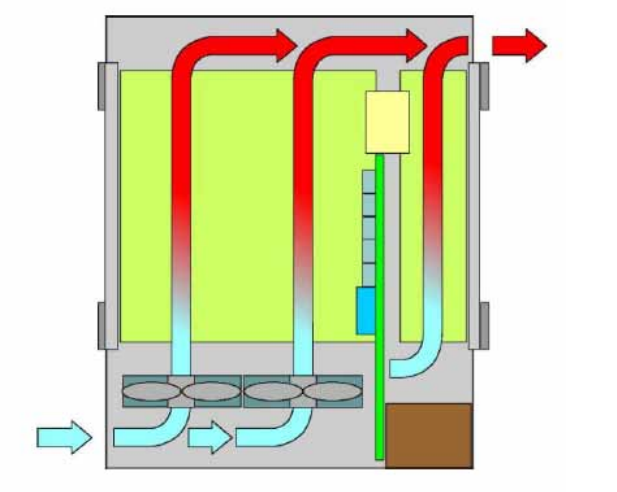

Figure 6- Typical Airflow in an ATCA Shelf [5]

Along with the recommendations are hard requirements, however, such as mandatory air filtering, which must trap over 80% of dust, and honeycomb or perforated metal screens for EMI control at the air intake and outlet. In addition, the Shelf should straighten airflow and provide roughly equal airflow to all of the Blades. In practice, however, it is commonly seen that Blades in the first and last slots receive reduced airflow.

Typical guidelines allow for an air temperature increase of 10ºC when the ambient temperature (T_a) is 55ºC, which can be problematic when working with higher powered boards. There are hard limits on temperature of the face plate of a board, with 70ºC being the limit with a T_a of 55ºC. The ATCA specification allows boards which consume up to 400 W, but less than 200 W is preferred. As the telecom industry pushes more and more powerful boards, however, we are beginning to see Shelves that are designed to support Blades over 300 W. Not far in the future, Shelves that incorporate sub-ambient refrigeration cooling or other alternative cooling techniques will become more common. One example of this would be the Therm-Jett air jet-impingement cooling system mentioned in the April 2011 issue of Qpedia [6].

The ATCA specification also defines the pressure drop across a board, with a maximum of 49.8 Pa (0.2" H_2O) at 30 CFM. The preferred pressure drop is 37 Pa, and if the pressure drop is too low, baffles must be added to the board to restrict air flow. Likewise, if a board is removed from a Shelf, a dummy board with baffles must be inserted into the empty slot to prevent excess air bypass around active cards.

This introduction to ATCA standards should be seen as a starting point, and is not comprehensive by any means. The full standard is available from PICMG [1] and is indispensable to anyone working with ATCA compliant components. In addition to the mechanical aspects touched on here, specifics for platform management, electrical design and other topics are laid out.

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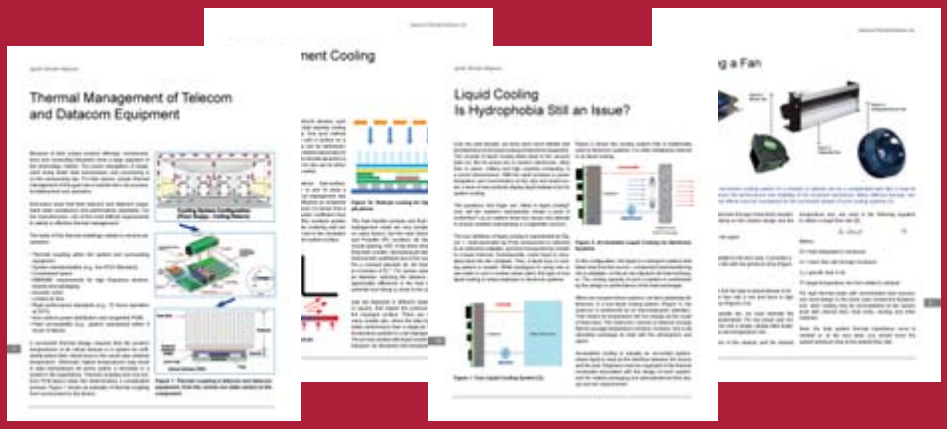

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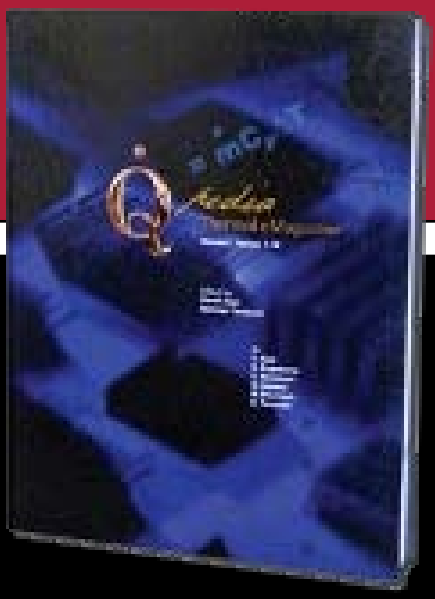

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Miniature Refrigerator

For A Laptop

As integrated circuits (ICs) have to provide increased functionality and computational power through a greater number of transistors in smaller and smaller packages, the removal of the heat dissipated by these electronic chips has become a serious challenge in the design of portable and other space-limited electronics devices. The cooling of these electronic chips in notebook computers is especially challenging due to the notebook's small footprint. Currently, heat pipes, as shown in figure 1 [1], are used to transport the heat from the high power components to a remote heat exchanger. The heat is then dissipated to the air passing through the remote exchanger. However, the heat dissipation using a heat pipe is approaching an asymptotic limit for the size restrictions of a notebook-shape form.

Figure 1 - Heat Pipe Cooling in Existing Notebook Computer [1]

Alternative cooling approaches have been investigated to achieve the required dissipation rates, while satisfying the required reliability and cost considerations. These methods are thermoelectrics and refrigeration. Given the small cooling capacity and low efficiency of thermoelectrics, a refrigeration system is the only viable method to further increase the heat dissipation of high power components in notebook computers.

Refrigeration cooling allows high heat flux dissipation at low junction temperatures, which will increase microprocessor performance at lower operating temperatures and increase chip reliability. However, refrigeration cooling also increases the size, complexity and cost of the cooling system. The complexity would increase the uncertainties in the system reliability.

Vapor-Compression Refrigeration system:

A basic vapor-compression refrigeration system consists of four major components: an evaporator, a compressor, a condenser and a throttling device. Figure 2 [2] shows a schematic of a vapor-compression refrigeration system. The main heat transfer mode of the vapor-compression refrigeration cycle is evaporation/condensation of the refrigerant.

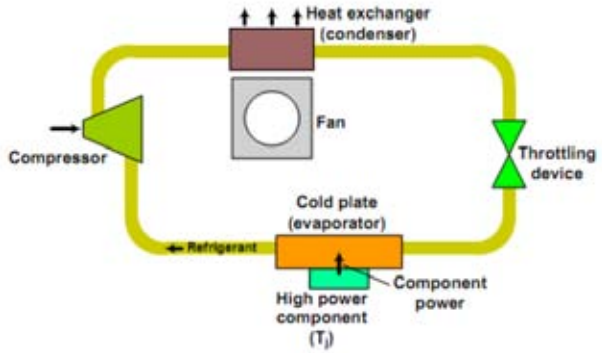
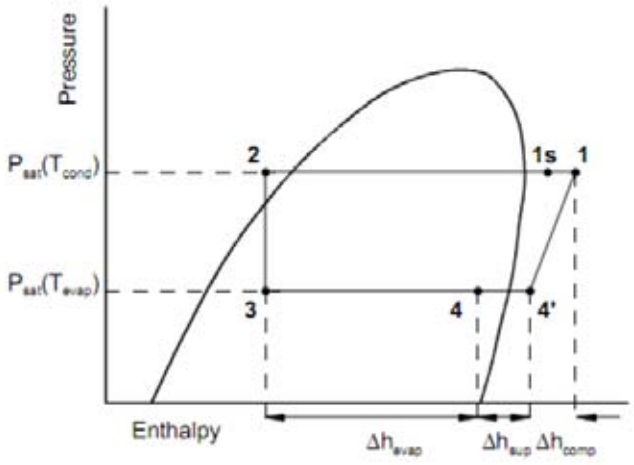


Figure 2 - Vapor-Compression Refrigeration System Schematic [2]

When the refrigerant enters the evaporator, it evaporates due to the low pressure and absorbs heat from the evaporator at a constant temperature. Then, the vapor refrigerant travels through the compressor, which increases the pressure of the refrigerant. After the compressor, the vapor refrigerant condenses in the condenser due to the high pressure and

rejects heat to the condenser at constant temperature. The refrigerant then travels through a throttling device, which reduces the liquid refrigerant pressure. The low pressure liquid refrigerant re-enters the evaporator and restarts the cycle. Figure 3 [2] shows the thermodynamic state point diagram of a vapor compression cycle.



State point	Location
1	Compressor outlet/condenser inlet
1s	Compressor outlet, isentropic
2	Condenser outlet/capillary tube inlet
3	Capillary tube exit/evaporator inlet
4	Evaporator exit/superheater inlet
4'	Superheater exit/compressor inlet

Figure 3 - Vapor Compression Cycle Thermodynamic State Point Diagram [2]

For electronic cooling, the evaporator would be directly attached to the high power electronic chip, absorbing the chip's heat dissipation. The heat dissipation would be rejected to the ambient environment through the air-cooled condenser. Figure 4 [3] shows the schematic of the vapor-compression cycle within a computer.

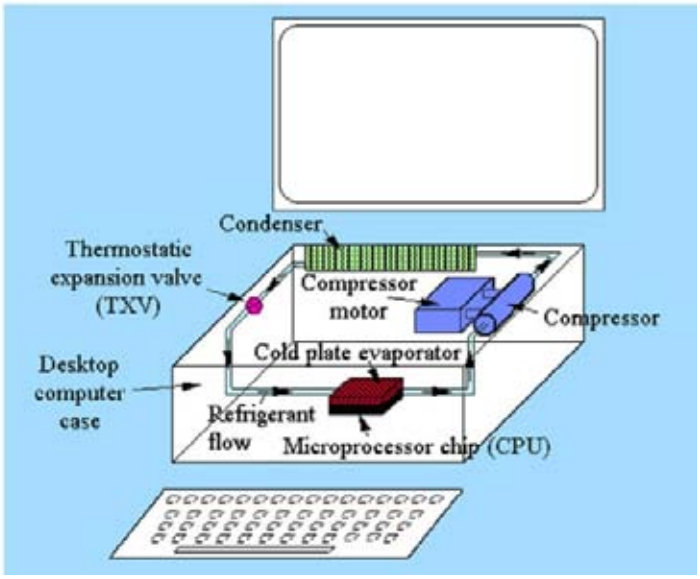


Figure 4 - Schematic of a Miniature Refrigeration System [3]

Recently, there have been a lot of studies that aim to further investigate the feasibility of the refrigeration system for electronics cooling. Studies of vapor compression systems and system simulation were directed at electronics cooling in laptop computers. One such study was conducted by Mongia, Masahiro, and DiStefano. The small-scale refrigeration system, within the study, included a compressor, cold plate, condenser and throttling device. These components were specially designed, such that the entire cooling system can be incorporated within a notebook form factor. Figure 5 [2] shows the schematic of the entire system with temperature and pressure measurement points.

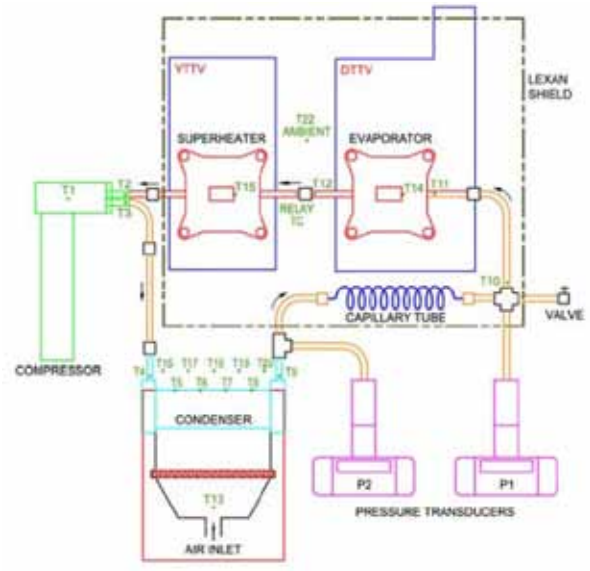


Figure 5 - Small Scale Refrigeration System Schematic [2]

Iso-butane was chosen as the working fluid. The cold plate and condenser contain microchannels to efficiently transfer heat to and from the refrigerant. Prototypes of each of the components were built and tested in order to assess their individual performance. Figure 6 [2] shows a complete form factor loop that was also built and tested to determine the system feasibility and overall performance. The test results, as shown in Figure 7 [2], show that this system can achieve a coefficient of performance (COP) > 2.25 at a moderate temperature rise. The thermal resistance of this system ranges from 0.28 – 0.7 °C/W. Figure 8 [2] shows the cooling loop within a notebook.

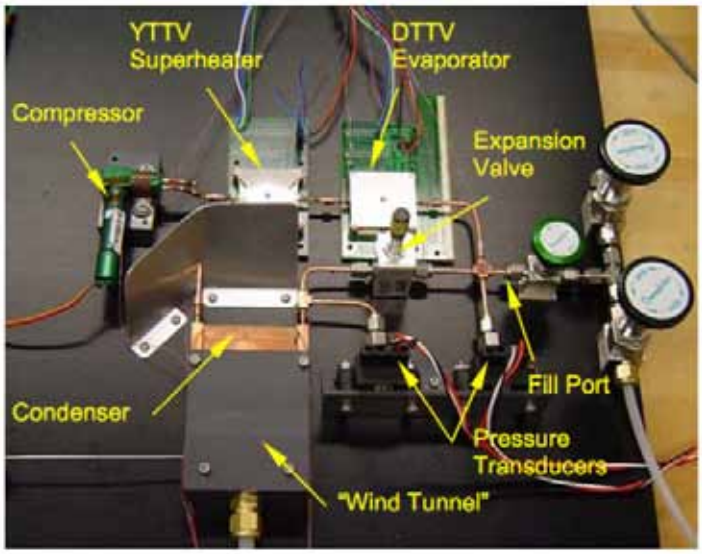


Figure 6 - Complete Small Scale Refrigeration Form Factor Loop [2]

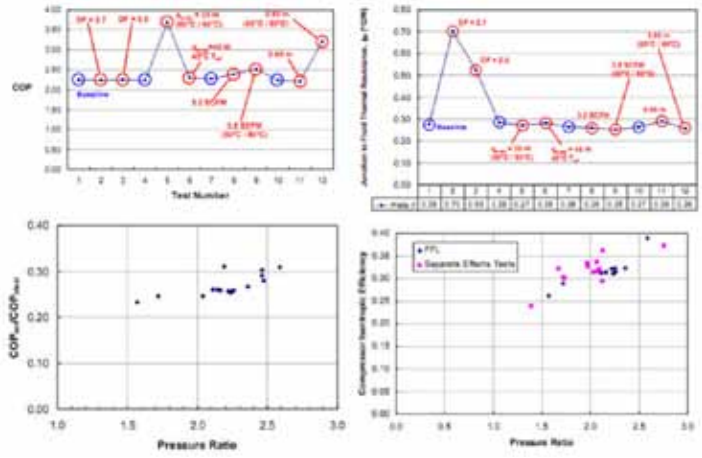


Figure 7 - Results from Small Scale Refrigeration [2]

Figure 8 - Small Scale Refrigeration System within a Notebook- Shape Form[2]

Miniature Scale Diaphragm Compressor (MSDC)

The researchers at Purdue have developed tiny compressors that pump refrigerants using penny-sized diaphragms, mainly of two contoured conductive planes that serve as electrodes. These planes are separated by dielectric insulation layers and a gas/refrigerant gap. As a voltage potential is applied between the electrodes, the electrostatic force deforms the diaphragm and pulls the diaphragm towards the electrode on the chamber wall. The contour of the compression chamber causes a progressive and continuous zipping action of the diaphragm until the membrane mates with the entire chamber wall. At the end of the compression strokes, the compression volume has almost zero dead space and the flexible diaphragm provides perfect rectification. Thus, the pressure of the refrigerant inside the chamber rises. The refrigerant flow in and out of the compressor chamber is controlled by suction and discharge flapper mini-valves. Target operational parameters for the miniature compressor are a heat removal of 200 W, pressure head of 750 kPa, pressure ratio of 2 and flow rate of 3000 ml/min. The targeted dimensions of the diaphragm compressor are 80 mm in diameter and 20 mm in height.

Although the new technology seems promising, there are still several challenges. One complication is that many diaphragms must operate in parallel in order to pump a large enough volume of refrigerant for the cooling system.

One possible solution is to stack the diaphragms within the system small enough to fit inside a laptop. The design can be optimized using computational methods, which enables the engineers to determine how many diaphragms to use and how to stack them, either in parallel to each other or in series. By stacking in one direction, the pressure might increase. While stacking in the other direction, the necessary volume would be able to be pumped. Another major challenge is to manufacture the compressors at a low cost.

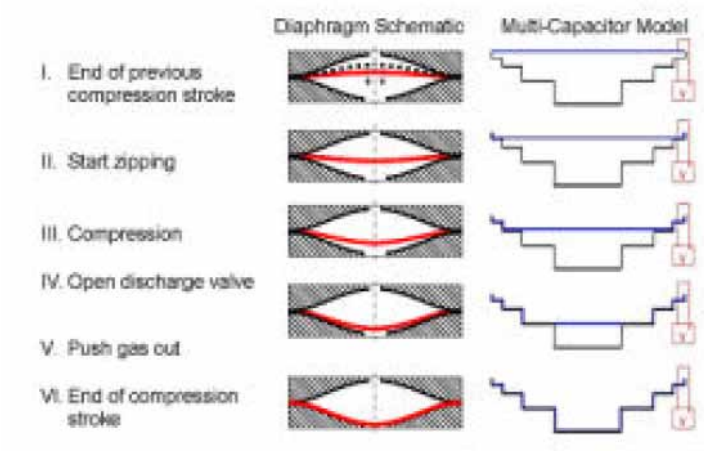


Figure 9 - Miniature Diaphragm Compressor Schematic [4]

Micro-channel heat sinks:

Another research project at Purdue is focusing on heat transfer in microchannel heat sinks, which circulate coolant through numerous channels about three times the width of a human hair. The micro-channel heat sink is a copper plate containing numerous grooves 231 microns wide – or about three times as wide as a human hair – and 713 microns deep. Figure 10 [5] shows Purdue researchers testing their microchannel heat sinks.

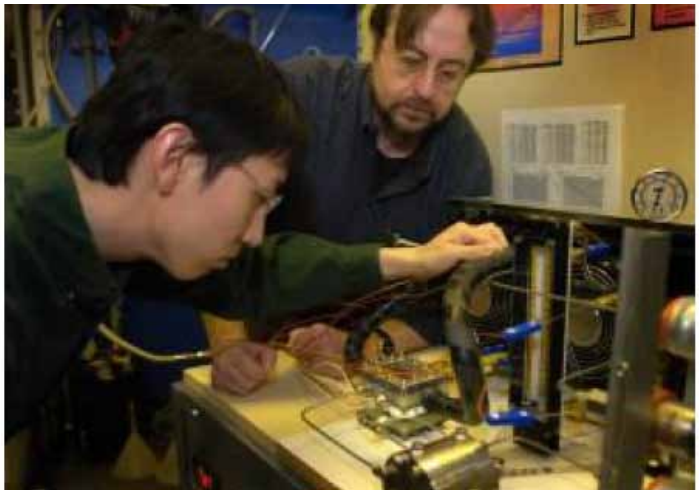


Figure 10 - Purdue Researchers Testing Micro-Channel Heat Sink [5]

Currently the researchers at Purdue are seeking to characterize and predict the enhancement due to boiling heat transfer provided by randomly roughen the surfaces in micro-channel heat sinks. Some results indicate that increasing the surface roughness by a factor of 3 yields a 30% enhancement in the amount of heat that can be removed while keeping the heat sink temperature constant. Further increases in surface roughness appear to be of little additional benefit.

There has been a lot of research in the feasibility and operational performance of small scale vapor-compression system. One promising area is the microchannel heat exchanger, which circulates coolant through numerous channels about three times the width of a human hair. Another promising area is a micro-diaphragm compressor. As the challenge of heat removal from more powerful electronic chips in smaller form shape increases, small scale vapor-compression system might be a promising solution.

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Thermal Simulation

and Management Of A 3D Stacked Chip

As new generations of electronic devices are required for more functions, connectivity, versatility, and less weight, their sizes keep on diminishing. These put enormous pressure on the chip design, device package and the thermal management of such devices. To put more functions into smaller size devices requires electrical and mechanical engineers to find intuitive ways to create new products.

System on Chip (SOC) refers to integrating all components of an electronic system into a single integrated chip. It may contain digital, analog, mixed-signal and, often, radio- frequency functions – all on a single chip substrate. A typical application is in the area of embedded systems, such as microcontrollers or smart phone chips. Stacked multi-chip design is an effective way to construct such a system on a chip module. Figure 1 shows a photo of a 3D stacked multichip module. This multichip module has four dies stacked on top of each other. The first die sits on the substrate and it is the largest in size. The second die sits on top of first die and they are separated by a silicon spacer. Its size is smaller than the first die. The third die sits on top of second die and bonds together with it. The forth die is smallest and is set on top of the third die. The electrical wires of all dies come down to the interconnectors on the substrate. In most cases, the interconnectors are extended outside through the conventional ball grid array (BGA) on the other side of substrate.

The advantages of using multi-chip module packaging includes:

1. Increased package density and performance, reduced chip size and weight
2. Added value on high-speed designs, improved signal integrity and assembly
3. Improved interconnection performance
4. Reduced chip restate area and overall power
5. Reduced board area and routing complexity at the next level.

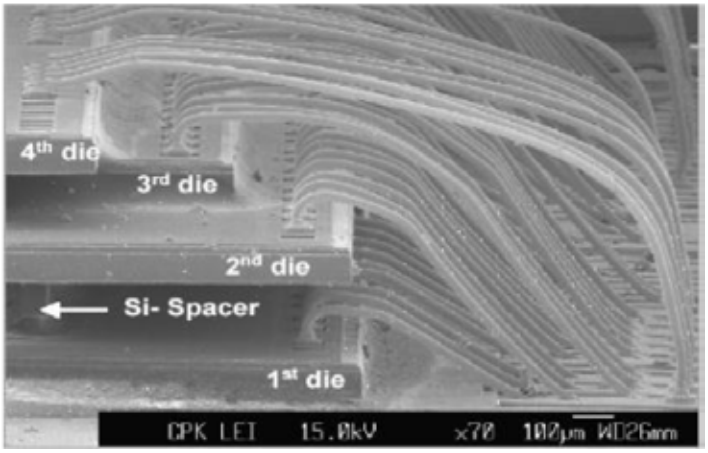

Figure 1- 3D Stacked Multichip Module [1]

The challenges of using multi-chip module packaging include:

1. Package parasites often affect signal matching, noise coupling and attenuation
2. Requires comprehensive 3D electromagnetic and mechanical analysis
3. Chip size, placement and thickness of interposer can affect the thermal stresses
4. Differences in the coefficients of thermal expansion coefficients result in differential thermal strain that induces stresses
5. Possible delamination and voids provide large thermal resistance and cause thermal problems in vertical stacked die package
6. Thermal management of multi-chip structure is difficult

For the mechanical and thermal engineer, challenges 3-6 are major concerns. From the point of view of thermal management, the prediction of the thermal resistance from dies to ambient and the temperature distribution in multiple dies is the main focus. Reducing the die junction temperature is, however, the ultimate goal.

Cumulative structure function gives the sum of the thermal capacitances C_Σ (cumulative thermal capacitance) as a function of the sum of the thermal resistances R_Σ (cumulative thermal resistance) of a system, measured from the point of excitation towards the ambient [2]. Figure 1 shows one example of the cumulative structure function.

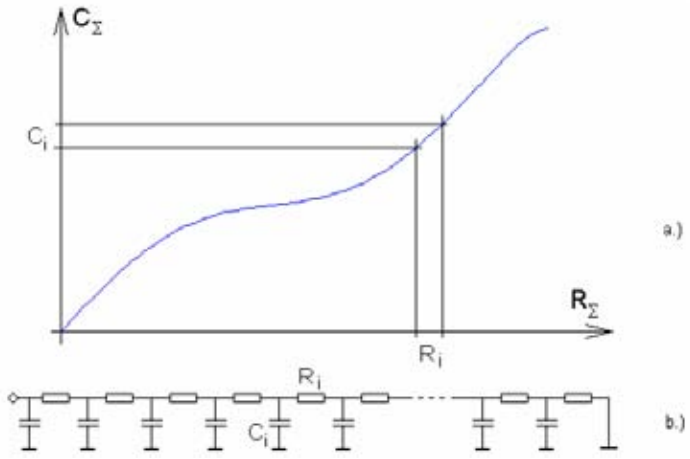

Figure 2. The Cumulative Structure Function and the Related Cauer Equivalent Circuit [2]

The differential structure function is defined as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance,

$$\mathrm{K}(R_\Sigma) = \frac{dC_\Sigma}{dR_\Sigma} \qquad (1)$$

For a dx wide slice of single matter with cross section area A,

$$dC_\Sigma = cAdx \qquad (2)$$

and,

$$dR_\Sigma = \frac{dx}{kA} \qquad (3)$$

where *c* is the volumetric heat capacitance and *k* is the thermal conductivity.

The *K* value of the differential structure function is,

$$\mathrm{K}(R_\Sigma) = ckA^2 \qquad (4)$$

The value *K* is proportional to the volumetric heat capacitance *c*, thermal conductivity *k*, and to the square of the cross sectional area *A*. As it is stated by Rencz and Székely in their paper [2], this function provides a map of the square of the heat current-flow cross section area as a function of the cumulative resistance. In these functions the local peaks indicate reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. More precisely the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform.

Rencz and Székely investigated a chip with three stacked dies by numerical simulation [2]. One quarter of the investigated pyramidal structure is illustrated in Figure 3. The size of the bottom die was 14x14 mm (7x7 in the ¼ simulation), the die size in the middle was 12x12 mm, and the size of the top die was 10x10 mm. The thickness of all the die and the glue layers were 0.035 mm. The considered thermal conductivity and volumetric thermal capacity values were 156 W/m.K and 1.6×10^6 W.s/m^{2}K for the silicon, 1 W/mK and 1×10^6 W.s/m^{2}K for the glue layers. The heat dissipating area is located in the middle of the top layer and the considered heat transfer coefficients were 6000 W/m^2.K on the bottom and 100 W/m^2.K on the top. The main heat flux is transferred to outside through the bottom of the package.

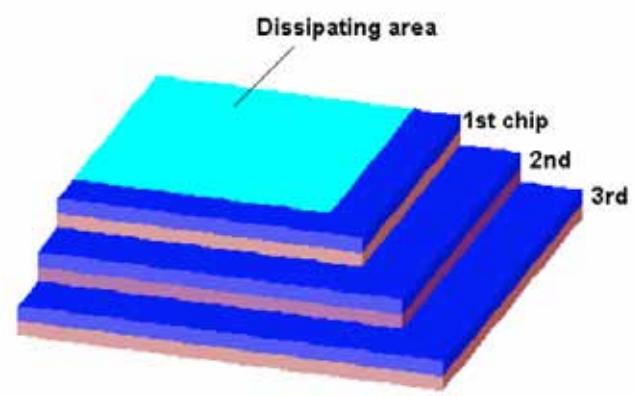

Figure 3. The Investigated Pyramidal Structure [2]

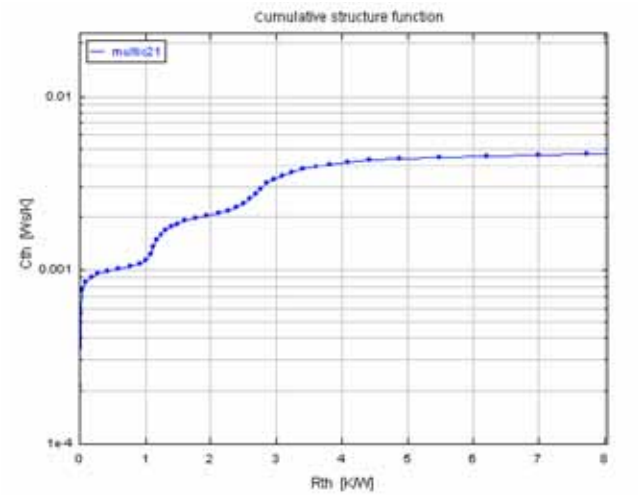

Figure 4. The Cumulative Structure Function of the Pyramidal Structure

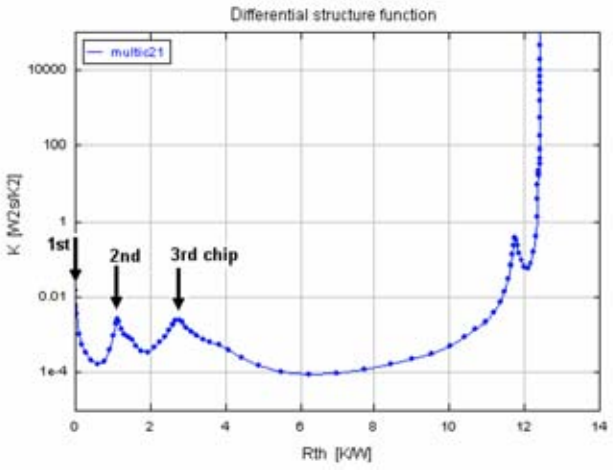

Figure 5. The Structure Function of the Pyramidal Structure [4]

The simulation results of Rencz and Székely's study [2] are shown in Figure 4 and 5. Figure 4 shows the cumulative structure function and Figure 5 shows the differential structure function of the Pyramidal structure. The thermal resistance and thermal capacitance values of each die can be read and calculated directly from the above figures.

To model the 3D stacked die structure analytically, compact *RC* model can be used. Figure 6 shows one example for a chip with 2 stacked dies. By using such model and die resistance obtained for structure function curve, engineers can easily predict the die temperature at different electrical loads.

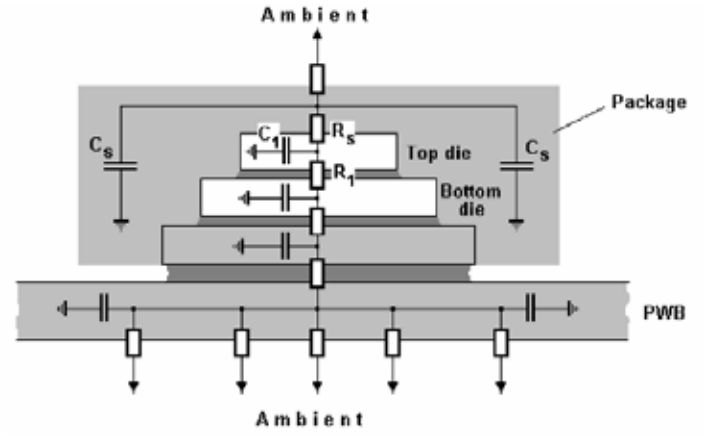

Figure 6. Compact Thermal Model of Package with 2 Stacked Dies [3]

The thermal simulation and modeling of 3D stacked chip are essential to understand the parameters and material properties that affect the thermal resistance and die temperature. But to solve the ever-growing problem of increasing heat flux load, innovative methods have to be used to remove heat of the dies and alleviate the die temperature.

The current and future cooling technologies for stacked die structure include:

1. Thermal vias and inter-plain heat spreaders
2. Single phase microchannel liquid cooling
3. Two-phase microchannel liquid cooling

The thermal vias provides the dies with thermal paths to heat sink or cold plate. The inter-plain heat spreaders smooth the temperature in the die and reduce the hot spots. They also help to transfer the heat to the case. The single-phase/two-phase liquid-cooled microchannel can be directly etched on silicon wafer by using same technology to make chips. So the microchannel can be integrated in 3D stacked die structure. Due to its miniature channel size, microchannel heat sinks can achieve extreme high convection heat transfer coefficient and low thermal resistance. Figure 6 shows a 3D stacked die with integrated liquid-cooled microchannel heat sink.

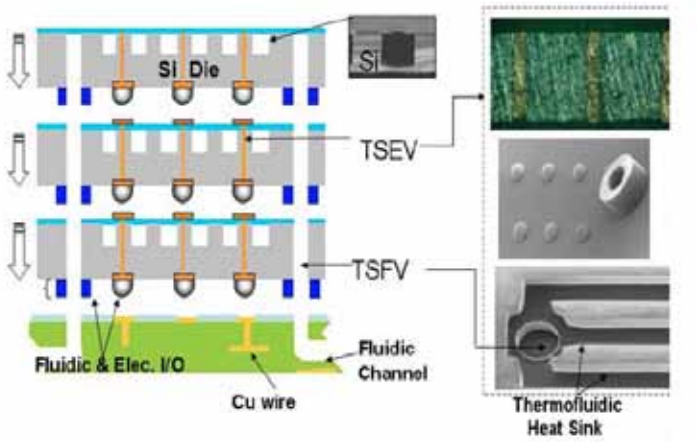

Figure 7. Schematic of 3D Stacked Chip with Microchannel Heat Sink [4]

For the low power 3D stacked die chip, the traditional method of cooling by using air-cooled heat sink and PCB board to dissipate heat is still valid as long as die junction temperature is below specification limit. Using better substrate and thermal via to smooth the temperature within multiple dies will reduce the peak junction temperature and alleviate stress between different dies. For high power 3D stacked die structure, the air-cooled method will reach its limit in the near future. The integrated cooling like liquid-cooled microchnnel heat sink shows great potential to solve the problem. But great deals of problems have to be solved before the start of the first real application of integrated liquid–cooled micrchochannel heat sink on chip.

The migration from air-cooling to liquid-cooling is not an easy task, especially on chip level. However, the integrated liquid-cooled microchannel can dramatically reduce the chip junction temperature for stacked dies, it will enable the chip to reach faster speed, have more functions, and still maintain smaller size.

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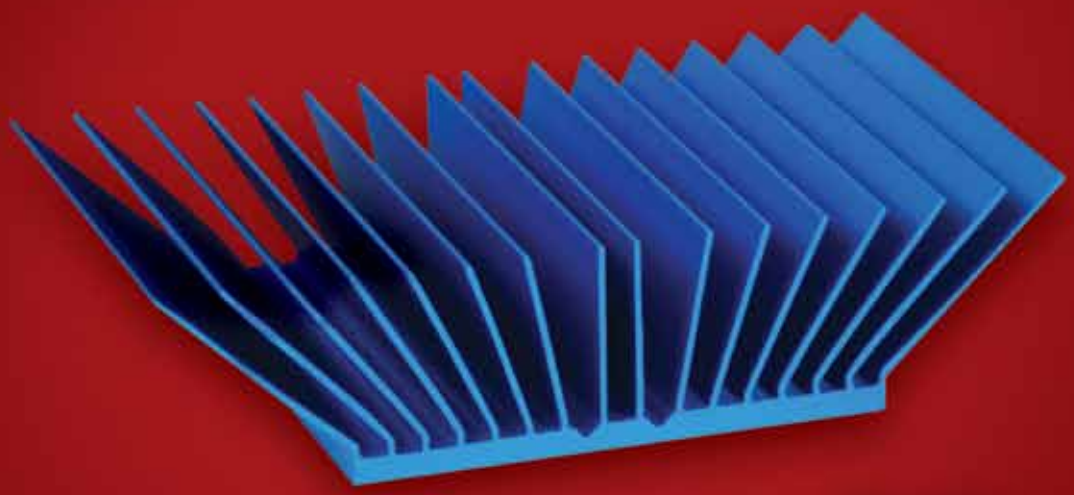

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JEDEC: Review Of Standards

On Compact Thermal Modeling

At the time when a gallon of gas was $.25 and the integrated circuit was deemed “invented”, an organization was formed known as JEDEC. The Joint Electron Devices Engineering Council is now made up of more than 3,000 volunteers from nearly 300 companies around the globe. The 50+ committees have a common vision: to create an evolving set of standards to ensure product interoperability, reduce cost and time to market. As a result, companies can base their designs on a set of standards and focus more on R&D. The resulting benefit is less time invested on product invention and more on innovation.

To maintain consistency with **Qpedia**, this article will focus on the thermal management of electronics and the JEDEC standard JC-15: Thermal Characterization Techniques for Semiconductor Packages. The scope of JC-15 includes the standardization of thermal characterization techniques, both testing (JESD51) and modeling (JESD15), for electronic packages, components and materials for semiconductor devices. For a closer look at standard JESD51 and the Thermal Measurement Methods of an Integrated Circuit, please look through the **Qpedia** archives and review an article in the June, 2007 issue titled: “Understanding the JEDEC Integrated Circuit Thermal Test Standards”.

The electronic industry has evolved such that new components are outperforming their predecessors. Packages are outputting more power, yet getting smaller in size, and operating at increasing temperatures. As we know in Thermal Engineering and as a Provider of Heat Sinks at Advanced Thermal Solutions, insuring that components are operating within the specified range is usually the last thing thought of when bringing new products through the design phase. These are highly 3D problems; insomuch as, in addition to the power of the devices, there can be increases in temperature due to the environment such as airflow characteristics, thermal coupling of neighboring devices, system altitude, etc. All possibilities must be taken into account when looking at how the entire system will operate.

When looking at a system, the greatest points of concern are the Junction Temperatures (T_j). As defined by JEDEC: “Absolute maximum rated junction temperature is the maximum junction temperature of an operating device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology” [1]. Figure 1 shows the junction location and an example of how a semiconductor can be packaged and installed onto a PCB.

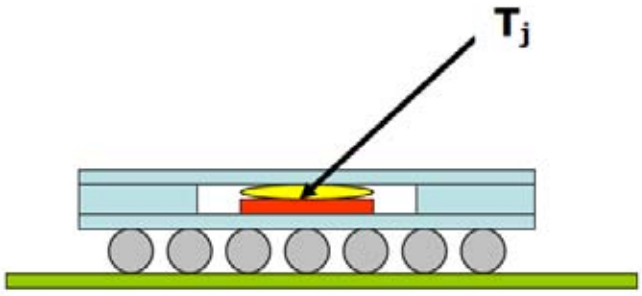


Figure 1 – Package Attached to PCB via BGA

During operation, The T_j must be monitored and maintained within the range specified by the device manufacturer. This is because temperatures outside the range speed up chemical reactions and accelerate changes in materials. This produces distortion stress on the junction between

two materials with different expansion rates. If this occurs repeatedly, material fatigue arises, causing failures such as hermetic seal damage, die bond adhesion damage and bonding wire opens. In addition, if the device is used with improper connections, the heat generated from the equipment or element can accelerate the temperature change and affect the product in an accelerated manner. [3]

The ranges differ per application; for example, the temperature range of a Xilinx Spartan -6 FPGA is:
C = Commercial (T_j = 0ºC to +85ºC)
I = Industrial (T_j = -40ºC to +100ºC)

Xilinx denotes this range in the item number by ending with a "C," or an "I." Check your own device manufacturer for the operating range for your application i.e., Commercial, Industrial, or Military.

For users to maintain a safe T_j, we must know the semiconductor's thermal resistance. Due to the fact that semiconductors need to perform in a wide array of environmental (surroundings, mounting, etc.), electrical (power levels, currents, voltages, etc.) suppliers must adhere to a standardized approach to defining the thermal resistance. It is by these means that both the manufacturer and the user can determine an accurate T_j.
Thermal modeling is constantly becoming more significant in the characterization of components and for predicting T_j for standard testing, as well as within the applications environment. The resulting data can be used by design engineers in evaluating the package itself, its reliability and to analyze the thermal performance of the entire system.
Due to the complexity of system level analysis, engineers would sometimes be constructing simulations with a lack of information. This resulted in an increased time investment to create an accurate model. Because of this, JEDEC decided that it made more sense for the suppliers themselves to characterize their own products for end users. There are several benefits to this approach. One major benefit is that the suppliers protect themselves by ensuring the accuracy of the thermal performance of their products and models released to their customers. In addition, if the models were said to be performed by the user, the supplier would lose any control over the accuracy of the data resulting from simulation.

JEDEC has introduced to the standards, Compact Thermal Models (CTM), to insure accuracy and compatibility throughout the industry, while providing a way for suppliers to share data effectively with global customers. A CTM is a way to "hone— in" on the component package and achieve a high level of boundary condition impedance (BCI), so that the thermal behavior of that component can be supplied for system level simulation. There are two methods defined by JEDEC, they are: The Two Resistor Model, and The DELPHI Model. These models are described below and are illustrated in Figures 2 and 4; but, first, let's look at the properties and assumptions that were made when creating these models:

Properties:
• Limited Complexity (10's of Nodes)
• Vendor/Software Neutral
• Adaptable to mainstream conduction codes for package-level thermal analysis
• Capable of insertion into standard numerical codes for system/board-level analysis
• Absolute BCI property is when CTM calculates chip temperature in all possible environments in agreement with results of detailed model calculation
• Fully documented, nonproprietary

Assumptions:
• Package contains single IC with each node representing a single temperature region
• Package mounted to a PCB
• Heat flows from the chip package to the:
– Top surface to ambient fluid or heat sink
– Side surfaces to ambient fluid
– Bottom surface / leads to PCB
• Thermal resistor networks are used to represent heat flow paths
• External surfaces can either be:
– Considered isothermal and represented by single nodes
– Subdivided into isothermal regions with corresponding nodes

As engineers, we can apply the Two-Resistor Model at different points of the design process. At first, the model may be used as an upfront calculation to see how the component/package may behave. Further into the design process, the model may be assimilated into a more detailed model using Computational Fluid Dynamics (CFD) software.

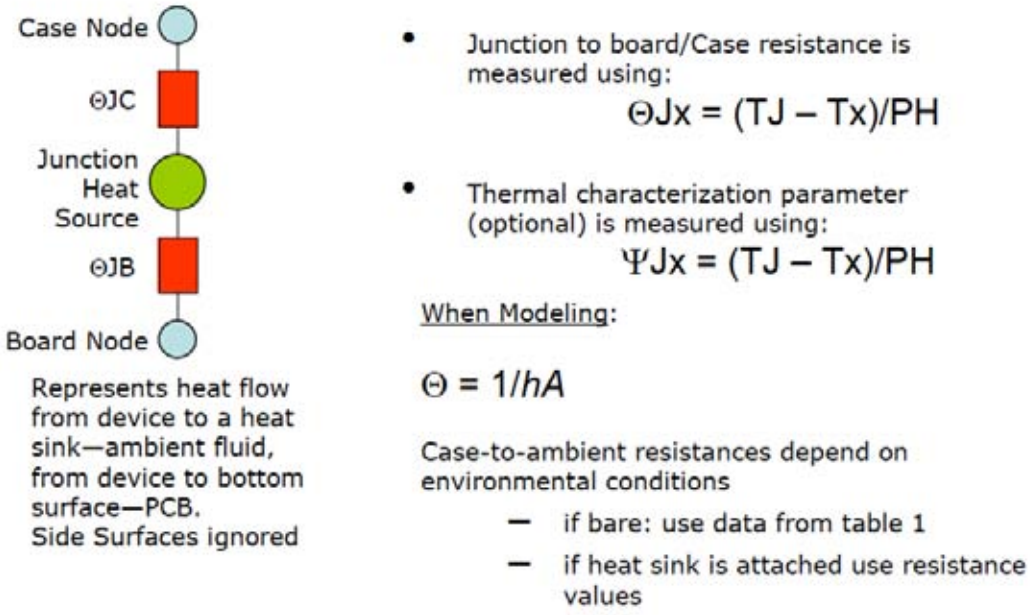


Figure 2 - Two Resistor Model

Cooling Regime	Approximate Heat Transfer Coefficient Range (W/m^2K)
Natural Convection, Air	2—30
Forced Convection, Air	15—3000
Forced Convection, Water	200—10,000
Pool Boiling, Water	3,000—50,000

Table 1 - Typical cooling regimes in electronics [4]

The Two-Resistor Model consists of three nodes connected by two thermal resistors. These represent the measured values of the Junction - Board (Θ_{JB}) and Junction - Case (Θ_{JC}) resistances as seen above, with the Board Node considered in direct thermal contact with the PCB under the package and the Case Node in direct contact with the environment atop the package. Typically, what is in contact with the top of the package is air or a thermal interface material in conjunction with a Heat Sink as seen in Figure 3. A heating power is then applied to the Junction node. In this model the heat flows in only two directions. No heat flow through the sides is accounted for.

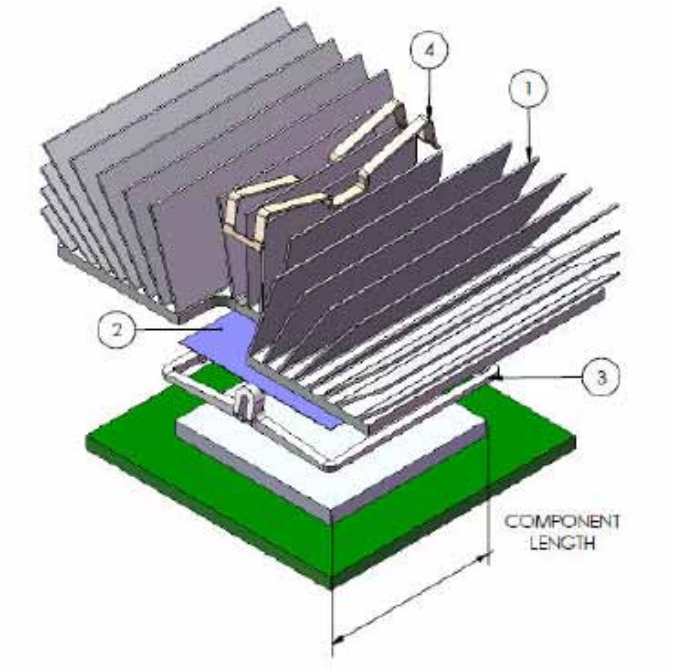


Figure 3 - maxiFLOW/superGRIP™ Heat Sink with Thermal Interface Material

As noted, care should be taken because the model doesn't consider environmental conditions, and these must be specified by the engineer at the Case and Board nodes. Furthermore, the error bounds cannot be determined from the generation of the model. They may be derived from comparing the engineer's predictions with data from actual tests.

As technology has evolved, the use of 3D simulation tools has become nearly standard. Using programs such as CFDesign™, and 6sigmaET™ can solve both the solid and air portions of the system directly. This is done by solving the Navier- Stokes equations which govern fluid flow and heat transfer. There is error in this method as well, as the program has to converge to a number. When setting up the CFD tool, care should be taken to ensure the correct interaction it will have with the surrounding flow. This is done by maintaining the physical geometry of the package. [4]

Table 2 shows the process flow for a thermal network and a 3D simulation approach to the Two-Resistor Model.

Conduct the ΘJB and ΘJC tests and extract metrics.	Generate as close to actual size and profile
ΘJB unavailable	Use software to construct two-resistor network
Calculate and use ΨJB	Verify the correct heat dissipation is introduced
Report metrics, package power and geometry	Assign emissivities to all correlating surfaces
Height, exposed top area, area contacting PCB	Ensure that the sides are insulated so that heat is only transferred through the top and bottom of model
Report emissivity of exposed package surfaces	

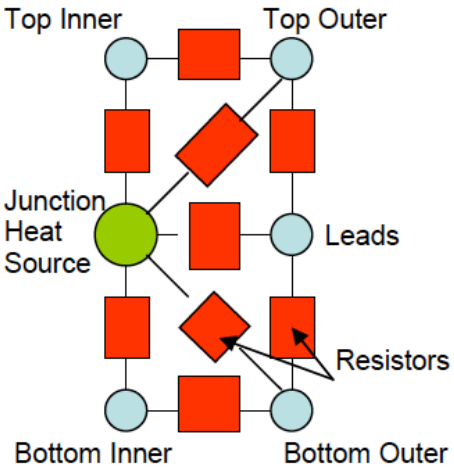
Table 2 - Thermal Network and 3D Simulation Methods

Even though less accurate, the intuitiveness and simplicity of the Two- Resistor model makes it attractive for engineers to construct. For a more complex and accurate approach, we shall look to the DELPHI project.

Much can be claimed by The DELPHI project. It is in fact, DELPHI (**DE**velopment of **L**ibraries of **PH**ysical models for an **I**ntegrated design environment) that coined the term "Compact Thermal Model" (CTM) and started the movement to establish standard methods of usage and sharing of component characterizations. After 1996, subsequent projects such as SEED (**S**upplier **E**valuation and **E**xploitation of **D**ELPHI) and PROFIT (**PR**ediction **OF** **T**emperature Gradients Influencing the Quality of Electronic Products) further develop publically the CTM, while members of each organization maintain their activity within JEDEC.

A DELPHI compact model is a thermal resistance network. This CTM is comprised of a limited number of nodes connected to each other by thermal resistor links (see Figure 4). With knowledge that the thermal problems are highly 3D, the heat flow within a component/package is represented in the model by a series of links. Network nodes are, by definition, each associated with a single temperature only. The nodes can be either surface or internal.

Surface nodes are associated with a physical region of the package surface defining the area of the node. In such a case, the nodal temperature represents the average temperature of the area allocated to the node in the actual package. Also, surface nodes must always have a direct one-to-one association with the corresponding physical areas on the actual package. Therefore, it is critical that they communicate with the environment in the same manner as the package. [5]



Temperatures averaged. Nodes communicate with each other. Surface nodes with environment, internals may have a heat source associated with them

- Objection function formulation:

$$F = \sum_{1}^{M} \left\{ W \left(\frac{T_{J,C} - T_{J,D}}{T_{J,D} - T_{Amb}} \right)^2 + \left(\frac{1 - W}{N} \right) \sum_{i=1}^{i=N} \left(\frac{q_{i,C} - q_{i,D}}{Q} \right)^2 \right\}$$

- where:
- F objection function
- M # boundary condition sets ("38 set")
- W weight factor (.5 balances flux & temp)
- N external nodes
- TJ,C junction temperature compact model
- TJ,D junction temp detailed model
- TAmb ambient temp
- qi,C flux leaving ith node (compact model)
- qi,D flux leaving ith node (detailed model)
- Q total power applied to the junction

Figure 4 - DELPHI Model

The objection function is the difference between the detailed model and the compact model summed over the boundary condition set and a finite number of points within the component package. [5]

Minimizing the Objection function should result in a compact model that has a low error. Table 3 illustrates the generation flow for DELPHI model generation.

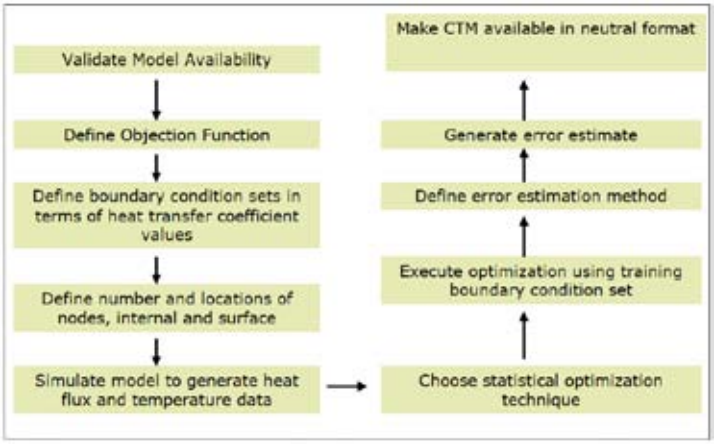


Table 3 - Steps in Generating the DELPHI Compact Model.

It is important to keep in mind that the availability of the DELPHI compact model does not eliminate the need for understanding the application in which the package is to be used. In other words, it is the user's responsibility to take into account the environment surrounding the package. The environmental conditions for the relevant application must be applied at the surface nodes as boundary conditions. [5]

There are a number of criteria that have been established to provide a comparison of the CTM methods. Table 4 shows the Criteria and the Application of it for each Model.

Two Resistor Model	DELPHI Model
• Is it test or simulation based?	
Test. The resistors are extracted from standard thermal tests or a validated model that simulates the test environment	Simulation. The resistor values are chosen by minimization of the Objective Function
• Does it contain an artifact from the test environment?	
Yes. There is a contribution due to heat flow through test board (note thermal conductivity—use 2s2p board)	No. Resistance for heat flow in the test board is neglected.
• Is there an error analysis included in methodology?	
No. Not in a two-resistor CTM	Yes, due to the statistical procedure used to extract optimum values for the resistors.
• Calculation of BCI and BCS Indices	
– Intended to provide comparison of accuracy between alternate methods	
– Supplier is requested to disclose calculated values of BCI and BCS Indices	

Table 4 - CTM Criteria – Comparison

The objective of the Compact Thermal Models, as described, is to simplify a component or package, verify its thermal performance and install the findings into a system, and perform simulations to determine thermal behavior within relevant applications. It has been in the best interest of suppliers to construct these CTMs and validate their products so that users shall have confidence in the capabilities of those products. The electronics cooling industry is much like fashion, in that: what may be successful today, will be unworkable or impractical tomorrow. JEDEC and its application of the CTMs are constantly evolving with the innovation of simulation tools, components and their applications. Within an ever changing marketplace, JEDEC standards advocate increases in reliability, interoperability, cost reduction and decreases in time-to-market for products within the microelectronics industry.

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Cooling News

New Products, Services and Events from around the Industry

Highly Thermally Conductive Epoxy System

Designed to help mitigate issues with tightly packed components and miniaturized electronic circuits, Master Bond's new EP21ANHT exhibits thermal conductivity over 22 BTU/in/ft²/hr/F° to provide high performance in demanding uses. The two-component adhesive, sealant, and coating has a convenient 1 to 1 mix ratio by weight or volume and offers room temperature and faster elevated temperature cures. Its coefficient of thermal expansion is 18-20 in/in x 10-6/°C, with a dielectric strength of >400 volts/mil, and a tensile shear strength greater than 1,000 psi.

Keratherm Softtherm®: 86/225

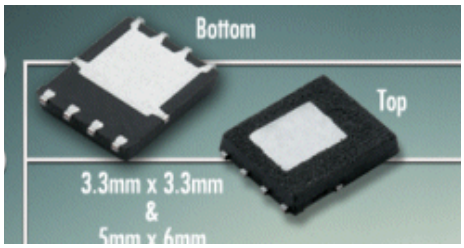
This new, single-layer Fiberglass-reinforced Softtherm® film is produced in thicknesses from 0.5mm to 5.0mm and has good self-adhesive behavior on both sides. Good thermal values and very good dielectric properties also characterize this film.

The film's ideal Shore hardness guarantees very good compressibility and good relaxation, along with vibration damping characteristics.

Possible Thickness: 0.5mm - 5.0mm

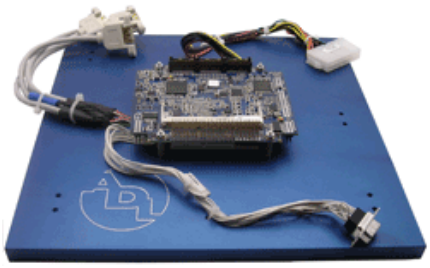
Applications:

- Heat Pipe Thermal Solutions
- Automotive Engine
- Control Systems
- Control Units



MOSFET package enables high power dissipation

The Dual Cool packaging for MOSFETs is a top-side cooling PQFN device that incorporates new packaging technology that enables additional power dissipation through the top of the package. The packaging features an exposed heat slug that delivers a significant reduction in thermal resistance from junction to the top of case, resulting in 60% higher power dissipation capability than standard PQFN packaging when a heat sink is mounted. The MOSFETs in the Dual Cool package are designed with proprietary PowerTrench process technology that enables lower RDS(on) and higher load currents in smaller package sizes. The MOSFET packaging, for top-side cooling, is available in Power33 (3.3 x 3.3-mm) and Power56 (5 x 6-mm) packaging options. The FDMS2504SDC, FDMS2506SDC, FDMS2508SDC, FDMS2510SDC (5 x 6 mm) and the FDMC7660DC (3.3 x 3.3 mm) suit synchronous rectifying MOSFETs for dc/dc converters, telecom secondary side rectification, and high-end server/workstation applications. (Ea/1,000: FDMS2504SDC, $4.14; FDMS2506SDC, $3.46; FDMS2508SDC, $2.70; FDMS2510SDC, $2.08; FDMC7660DC, $1.38 — available now.)



Highly Thermally Conductive Epoxy System Simulator features thermal, radiative cooling surface

The CS-100 Thermal Chassis Simulator provides a thermal mass and radiative cooling surface for passive cooling of ADL CPUs. The 100-in.2 chassis is used with its universal mounting pattern and is compatible with all of the company's PC/104 heat spreaders and pipes, regardless of the CPU. The product contains both M3 and 4-40 hardware, as well as standoffs to support 0.600- or 1.000-in. clearance spreaders. The thermal simulator is made from Blanchard-ground powder-cast plate aluminum. It has a surface flatness better than 0.001 in. across the entire face. The anodizing provides basic emissivity of ≤0.75 and represents the radiative area of an aluminum enclosure with 200-in.2 It is used as a development platform for proof-of-concept passive cooling systems. ($299 — available now.)

Fan provides 21-cfm air flow

The AG4015 fan measures 40 x 40 x 15 mm and features an impeller design that enables it to rotate at 15,000 rpm, and produce 21-cfm air flow. It provides static pressure of 0.92 in. of water while maintaining a 51-dBA noise levels. The fan is available with operating voltages of 5, 12, and 24 Vdc. It suits storage, networking, set-top box, game console, and power applications. Standard operating temperature ranges from 10 to +70C. Options include extended temperature ratings, IP-55 rated water protection, on-board PWM control, alarm output, tachometer output, and thermistor control. (Contact 561-241-6700 price and availability.)

iQ-200

iQ-200 is a new instrument from Advanced Thermal Solutions, Inc. that measures air flow, air temperature, surface temperature and differential pressure drop simultaneously. The instrument comes with 16 velocity channels, 12 thermocouples and 4 pressure transducers. All three functions are bundled in one instrument.

OVERALL DIMENSIONS
(D x W x H)
43 cm x 34 cm x 12.6 cm
(17" x 13.3" x 5")

NUMBER OF VELOCITY CHANNELS - 16

FLOW RANGE
0 to 50 m/s (0 to 10,000 ft/min)

NUMBER OF THERMOCUPLES
12 (J, K, T, and E types)

NUMBER OF PRESSURE SENSORS
4 (Differential)

PRESSURE RANGE
0 to 0.15 psi

SOFTWARE
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