The need for thermal management

- How big is the problem?
- What heat does to the circuit
- What happens if we ignore the challenge?
- How thermal design is tackled

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As our introduction says, thermal management is often not taken seriously, or even considered at all, so our first section focuses on what we are certain is an increasing need, and on the rationale for taking some action.

In this part of the presentation we are looking at the overall scope of the problem and the drivers, and in the following parts we will be considering what heat does to the circuit, then what happens if we ignore the challenge, and finally how thermal design is tackled.

How big is the problem?

- In some applications, quite severe
- Becoming more of a problem, and more widespread
- Happening at all levels from component to system

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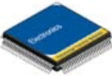
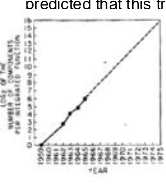
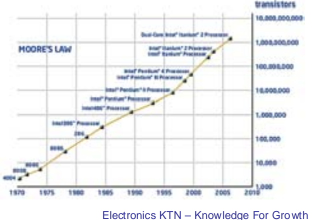
Just how big is the problem? Well not usually as dramatic as a burning heat sink, but in some applications the thermal problems can be quite severe, and the consequences of poor thermal management, or no thermal management at all, are becoming more of a problem and more widespread. The difficulties are happening at all levels, from the component right through to the large system.



Trends in power

- Increase in complexity (Moore's Law)
  In 1965, Gordon Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this tren





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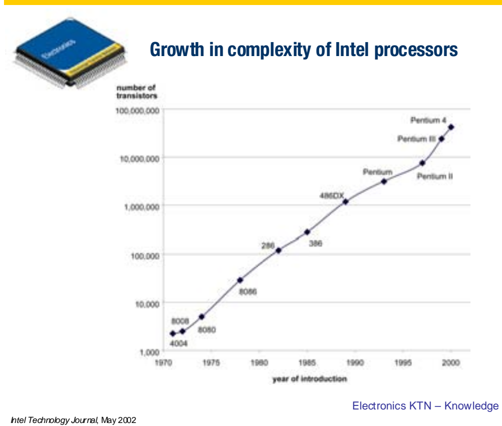
The problems of course are driven by the application, and in particular by the trends in power dissipation of key components. Much of that is due to the increase in complexity that we refer to as Moore's Law. In 1965 Gordon Moore of Intel observed that the number of transistors per integrated circuit had shown exponential growth, and he predicted from that that this trend would continue.

This is what his original graph looks like plotted on a logarithmic scale, and linearly extrapolated. He only took it to 1975, but in practice this trend has continued for a further 30 years, fuelled by technology advances that have allowed feature sizes to shrink by several orders of magnitude.

Growth in complexity of Intel processors



Intel Technology Journal, May 2002

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Moore's original projection was of course in terms of transistors, and way before the advent of the CMOS device, but his rule still holds, and can be seen very clearly in the growth of complexity of the resulting devices. Again, this is a linear graph on a logarithmic scale, which corresponds very nicely with the growth of power shown in the next slide …

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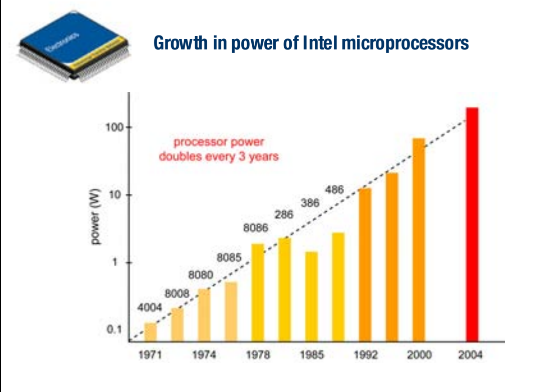
The need for thermal management

Growth in power of Intel microprocessors



Intel Technology Journal, May 2002

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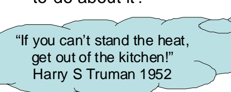
… which is again linear on a logarithmic scale, representing this time an exponential growth in power. This considerable increase in power is partly a result of complexity but has much more to do with clock speed.

Power consumption of digital circuits is related to the switching speed – the faster they go, the more heat is generated. My first 8086-based processor ran at only 4.7MHz (though this seemed fast at the time!) and over the following twenty years speeds increased to 3.8GHz, though the rate of increase now seems to have stalled. During the same period, power consumption increased to over 100W.

Processors get really quite hot!

- "If you can't stand the heat, what are you going to do about it?"



A British technician fried an egg using the heat from his PC's 1,500 MHz CPU. It took only 11 minutes!
The experiment used coins to replace the original heat sink.

Chip Scale Review, March 2003

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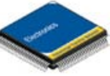
Processors get really quite hot, as you will know if you have ever touched the processor on your PC's motherboard. This shows what happened when a technician replaced the original heat sink with old copper coins and tried frying an egg. With a 1.5GHz processor, it took 11 minutes.

Flomerics distributed the news of this experiment, commenting that: "although intended as a piece of fun, this experiment underlines the serious implications of the thermal issues that Flomerics believes will become the limiting factor in chip design."

And these days Harry Truman's comment about thermal avoidance is unfortunately not something that an electronics equipment designer can take on board!



Exponential growth in power

- Increase in complexity (Moore's Law)
- Increase in speed
- Higher currents
  - present designs use V_{core} <1.5V
  - "the 45nm feature size will require as low as a 0.7V operating voltage with a maximum of 198W" (ITRS 2006)
  - 45nm microprocessors may require up to 200A

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The increase in speed and complexity has been accompanied by a reduction in working voltage. Earlier processors ran on 5V, which reduced to 3.3V, and present designs use a Vcore of under 1.5V, produced by local voltage regulation.

As the feature size has reduced, so has the operating voltage, and 45nm devices were predicted in 2006 to require as low as 0.7V. A more recent forecast is that a 45nm microprocessor may require up to 200A. This high current requirement is why so many package pins are dedicated to power and ground – typically 25% of all pins on a processor package. And this also has an indirect thermal impact, which becomes more important as the voltage is reduced, due to I squared R heating throughout the interconnection links.

Exponential growth in power

- Increase in complexity (Moore's Law)
- Increase in speed
- Higher currents
- Higher leakage currents
  - the 65nm challenge
    "a 65nm chip can lose as much as 60% of its power to sub-threshold leakage"

John Stabinow, Components in Electronics, May 2008 p.37

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But power is not just consumed during operation: there are also higher leakage currents as silicon devices get smaller. John Stabinow suggests that a 65nm chip can lose as much as 60% of its power to sub-threshold leakage. So a significant amount of power is being lost rather than consumed usefully, which adds to the thermal challenge.

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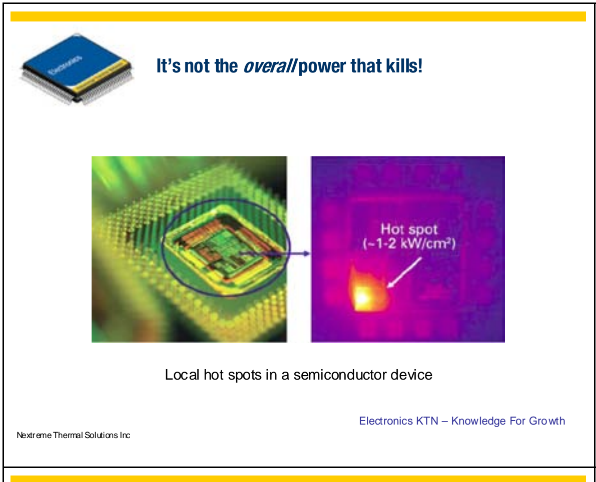
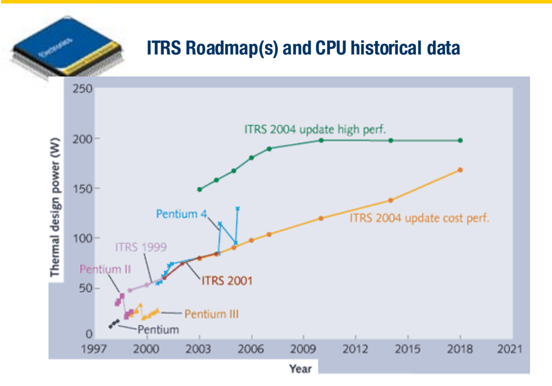
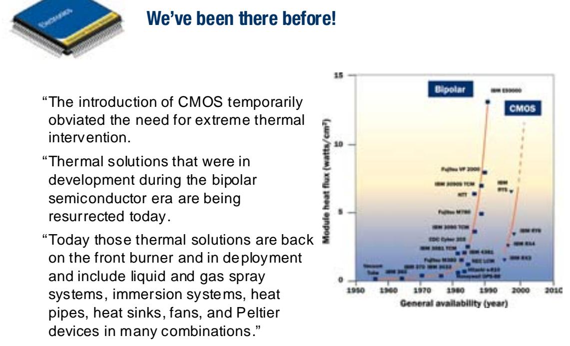
The need for thermal management

	We have to remember though that it is not the overall power that kills, but local hot spots within the chip. This photograph shows a Pin Grid Array, with a bottom-up chip, and with the lid on the underside removed to make the die visible. In this case, there is an uneven heat distribution, and a corresponding hot spot on the chip. The stresses induced locally will be quite considerable, and may lead to early failure.
	We've already seen the power creeping up inexorably, and this is reflected in projections such as this ITRS Roadmap, which shows continued significant rises, and a corresponding thermal management challenge. Of course, in these green-aware days, there are significant pressures to reduce power consumption, so reality may buck the trend. But we still have relatively high power and increasing power densities, and the need for thermal management remains.
	Of course, we have been there before, as Joe Fjelstad reminded us in a recent webinar to which we are privileged to put a link in this section. Those who remember the 1980s will recall the way in which bipolar technology became more competent, but at the expense of considerable increases in power. So a high-end system could take up a whole room, and there were significant thermal challenges.
	As Joe Fjelstad rightly comments, the speed increases from CMOS fuelled a move away from bipolar technologies, and "temporarily obviated the need for extreme thermal intervention". But of course that need was only pushed back some years, and engineers have been faced with the same challenges. And in many cases it's the same thermal solutions that were worked on in the last century that are now being used, including some very innovative combinations of technologies.

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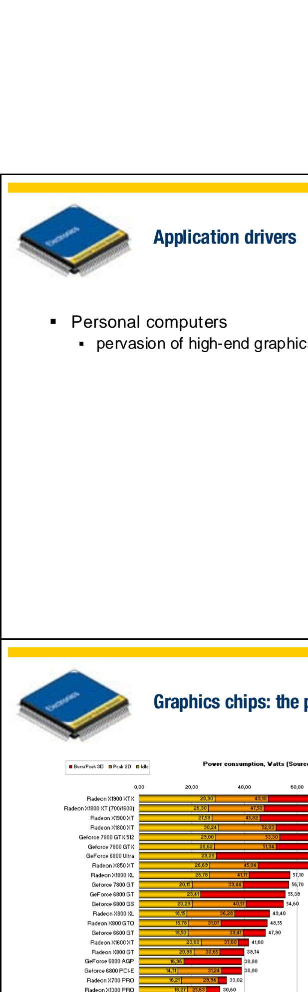

Application drivers

- Personal computers
  - pervasion of high-end graphics

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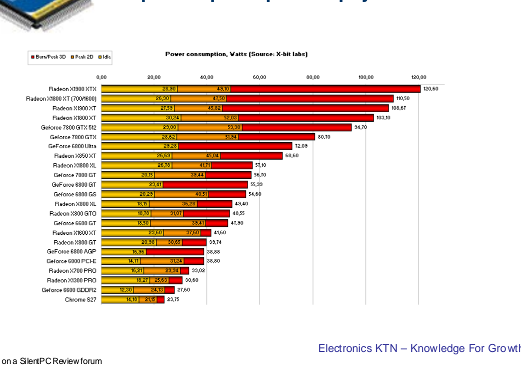
The technology itself is the source of the thermal challenge, but the technology also fuels the application, and in many cases the applications themselves are drivers for increased thermal management demands.

One such is the pervasion of high-end graphics. A colleague was telling me a few months back about a computer where he had upgraded the graphics, and in doing so took out the whole system because of over-temperature.

Graphics chips: the power of play!



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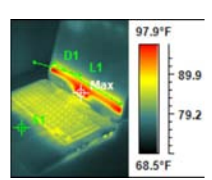
posted on a SilentPC Review forum

Computers frequently have specialised graphic chips which are processors in their own right, and consume at least as much power. This illustration, which was posted on a SilentPC Review forum, shows power consumption in watts for different types of graphics processor.

Whilst the idle power is significant, varying from 12–28W, what is alarming is the considerable increase during operation. Two-dimensional graphics have a lower demand, shown in orange, but the red bars show the peak power consumption when undertaking 3D graphics processing, and the more competent chips here are significantly high consumers of energy.

Application drivers

- Personal computers
  - pervasion of high-end graphics
  - laptops



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Not all computers are needed to work that hard, and significant power savings have been sought for computers made for laptop use. But even here, there will be some parts of the structure that get hotter than one might expect, and certainly laptop huggers will know the way in which the complete case warms up during use!

Application drivers

- Personal computers
  - pervasion of high-end graphics
  - laptops
- Mobile phones

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Another user of rechargeable batteries is the mobile phone, and this also generates thermal challenges …

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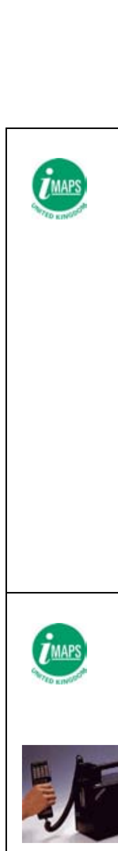
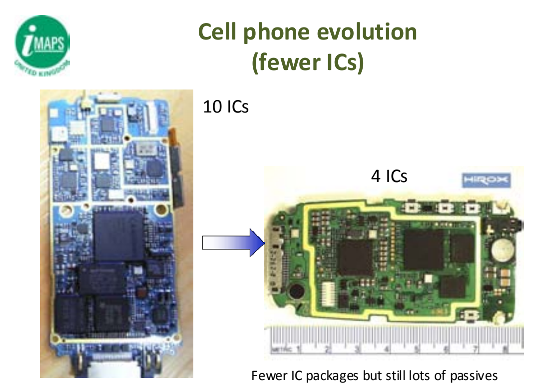
The need for thermal management

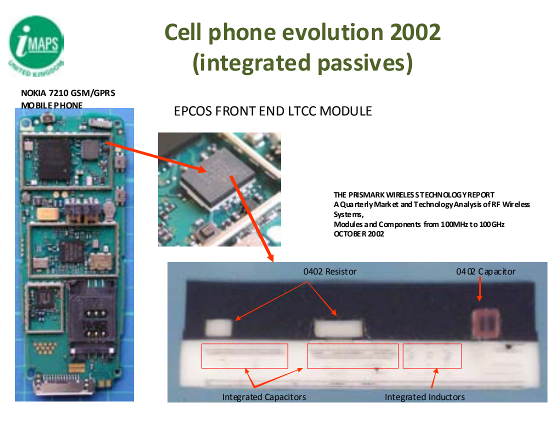


… though most of the advances made since this picture was taken in 1968 have more to do with size reduction than with thermal management.

It is only since the development of rechargeable batteries with an increased power to volume ratio that thermal management has been a significant issue.



As we move to simpler constructions, with fewer integrated circuits, we can't totally ignore thermal management, given that some sections of the circuit will be working as a UHF power transmitter.



The situation of course with these examples of extreme miniaturisation is that elements are becoming more complex, for example by the integration of components as indicated in this slide.

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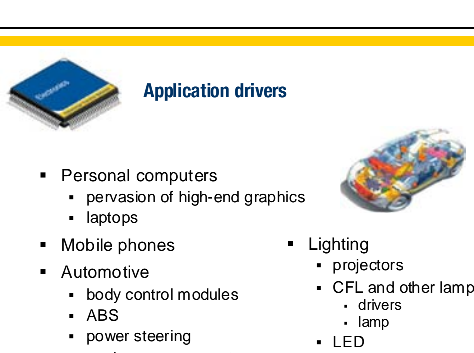
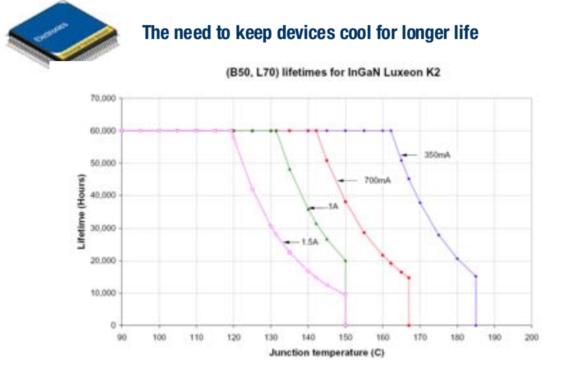
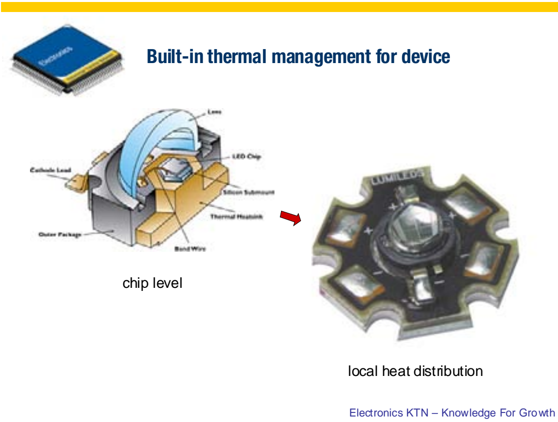


Another major user of electronics with special requirements is the automotive industry, where electronics are an increasing part of the cost of any vehicle, the reliability requirements are tight, and the environment is distinctly challenging, especially in under-bonnet applications.

There is a saying about “more heat than light”, and lighting is certainly an area where efficiencies are relatively low, and thermal challenges correspondingly high. One of our case studies concerns cooling for a projector unit, and most energy-efficient lamps, whether they are compact fluorescent tubes or light-emitting diodes, have significant heat dissipation to take into account.

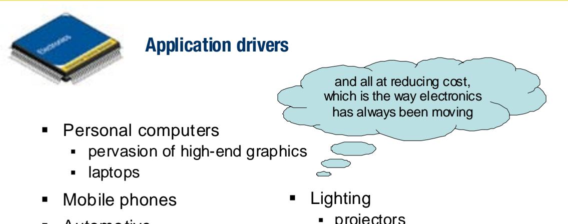


The reason for this is that, the cooler the devices stay, the longer they live before burn-out, a point that is made graphically in this extract from a Philips data sheet.



It is not surprising therefore that devices have thermal management considerations very carefully borne in mind throughout their design and development. We see here the LED device, mounted directly onto a metal heat sink that projects at the base of the package.

And this package is mounted on a special substrate that provides both connections and a means of spreading the heat. There will be more about this in a case study in Section 4.



Of course the final application driver, as with all electronics, is to provide functionality, performance and reliability all at reducing cost, which is the way in which electronics has always been moving.

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The need for thermal management

This shows the bipolar versus CMOS picture in its original format, with a picture of the IBM processor and some scary prices. We can get similar functionality these days for very much less money, and it is significant that the machines are almost becoming a throwaway item. And you will have heard of moves to make laptops available in the Third World at a very affordable price.

An increasing challenge

- Total power increasing
- Dissipation density increasing
- Driven by applications
  - telecoms

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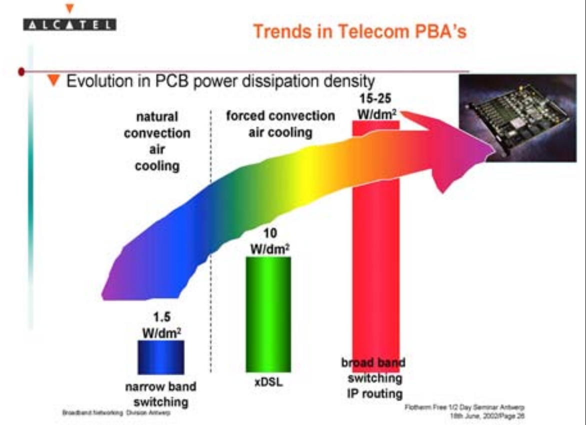
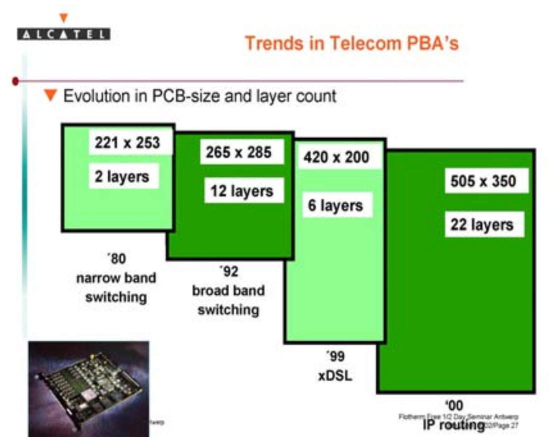
We have looked so far at the results of Moore's Law, and the technology and market drivers, and we have an increasing challenge in terms of both total power and dissipation density, again driven by applications.



If we take the telecoms market as an example. This graphic shows the development over the period from the late 1980s. The unit is watts per decimetre squared, in other words dissipation on a square of side 10cm. Even at the broadband switching and routing end, the 15–25W doesn't seem to be too much of a problem. Until, that is, you realise that the boards are considerably bigger than 100mm per side, and you can end up with a board dissipating almost kWs …



… because, at the same time, boards have been becoming larger and more complex. This large size, combined with a higher power dissipation density, gives a significant challenge of thermal management. The only positive here is that boards are becoming more complex, so have more layers and will be marginally better at spreading heat.

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The need for thermal management

An increasing challenge

- Total power increasing
- Dissipation density increasing
- Driven by applications
  - telecoms
  - data infrastructure — server farms

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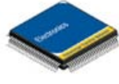
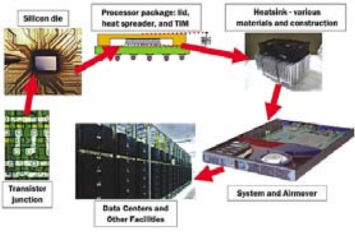
If we move from telecoms to data infrastructure we get a flavour of the overall problem when we have a whole facility to cool.



Design challenges at the data centre level



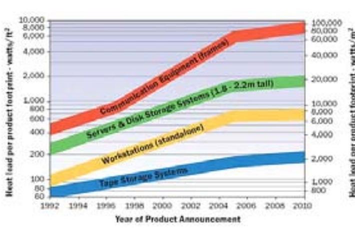
De Lorenzo and Opdahl, *Electronics Cooling*, February 2005

Electronics KTN – Knowledge For Growth

In the paper from which this slide was taken, De Lorenzo and Opdahl are focusing on the larger scale, and on keeping the room cool, but it is interesting that they show the problem starting right back at the individual transistor level.

This is a reminder to us that thermal design challenges run all the way through die design and semiconductor packaging, and through methods of heat management that involve both conduction and convection cooling. And of course the heat isn't lost entirely and ends up in the air-conditioning system for the data centre.

Design challenges at the data centre level



De Lorenzo and Opdahl, *Electronics Cooling*, February 2005

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The challenge is made significantly more difficult by the trends in heat density. This shows the heat load as a function of the footprint of the eventual product. Not only is the trend marked, but the cooling requirements are very significant.

An increasing challenge

- Total power increasing
- Dissipation density increasing
- Driven by applications
  - telecoms
  - data infrastructure — server farms
- Complicated by other changes
  - board size
  - layer count
  - specialised package design

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We have already seen that the size of the challenge has been complicated by related changes in terms of board size and layer count, and the complexities are added to by the continuing evolution of the semiconductor packages that are the source of the heat.

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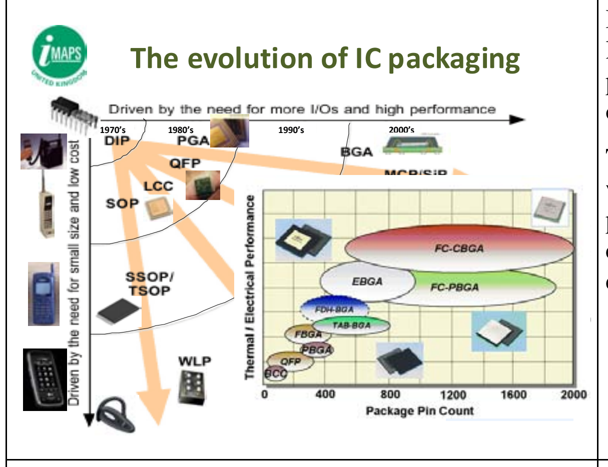
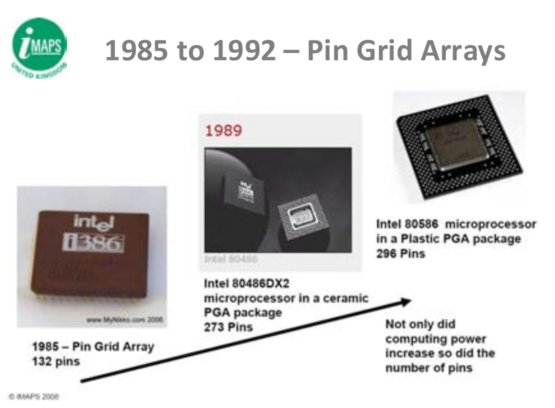
The need for thermal management



If we follow this two-dimensional graph from its origin in the top left-hand corner, which is a dual-in-line package, we see both packages of increasing complexity along the X axis, and devices of decreasing size down the Y axis.

The drivers depend on the application, and if we expand the inset, we can see another relationship which is between the thermal performance and the complexity as measured by the package pin count. Note that much of the thermal action is with area array devices …



… and it is worth looking at how these developed, first from a pin grid array …

… and then to various board grid array packages, that show significant advances in power density and sophistication. There are also structural changes, with the die bonded face-down to the board using flip-chip processes. Each of these designs has different thermal challenges!

Industry drivers & trends

- Miniaturisation is not just about silicon …
  - there's "more than Moore"

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In many ways, the heat generated by semiconductor devices will continue to be the largest part of overall product dissipation, but we must not forget that when it comes to making things smaller, it's not just about the silicon, and there is "more than Moore".

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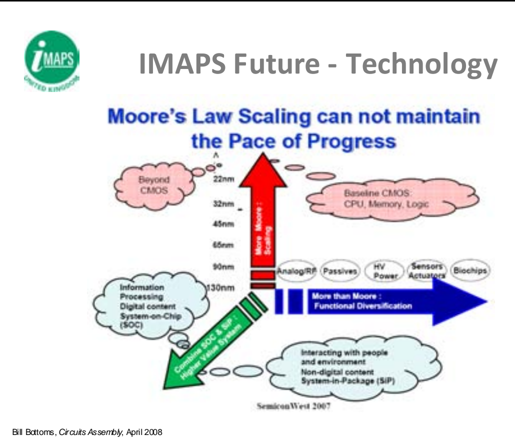

</td>
<td>Bill Bottoms makes the comment that we are nearing the basic physical limits of CMOS scaling, and suggests that new materials and device architectures in development will eventually provide a path to increased density, to increased performance and to lower cost, but that there will be a time lapse in their availability. Meantime, packaging innovations are taking up the slack, using both System-on-Chip and System-in-Package technologies.</td>
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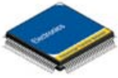
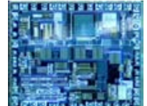


Industry drivers & trends

- Miniaturisation is not just about silicon …
  - there's "more than Moore"
- Several possible miniaturisation strategies
- System-on-Chip (SoC)
  - everything is integrated in silicon
  - high non-recurring expenditure
  - low cost in high volume
  - may be some performance compromises



Electronics KTN – Knowledge For Growth
</td>
<td>System-on-Chip, where all the functions are integrated into a single device, is a concept with considerable history. As with all such silicon, you have a choice of programming a ready-built system or "rolling your own", in which case there will be a high tooling cost. But the positive aspect is that the volume manufacturing costs are low, with just one die to make and assemble, and many fewer packages in the overall system.</td>
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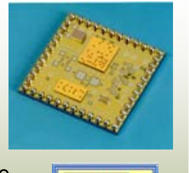
FLOMERICS Industry Drivers & Trends

- System-in-Package (SiP): a new paradigm
  - Embedded passives
  - Multiple active & passive die
  - Standard package outline
  - Stacked Die, modules, MCMs
    - Flexibility
  - Faster time-to-market
  - Lower non-recurring expenditure
  - Higher performance



ADEPT SiP

Changing Role of CFD in Electronics Thermal Design
</td>
<td>The System-in-Package has been described by its promoters in the glowing terms of "a new paradigm", although the concepts involved are far from new. The aim is to use the best of existing technologies, and group them together to give an overall product that can be on the market faster, is economic in relatively small volume, and has none of the performance compromises that System-on-Chip may show.</td>
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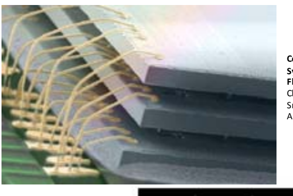
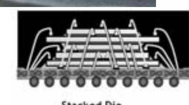
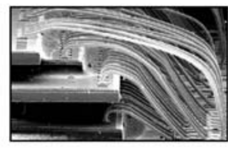
Stack packages / wire bond



Convergence and Connectivity 2003
System in Package:
Flexibility in Integration
Chris Scanlan
Sr. Director, System in Package
Amkor Technology



Stacked Die FBGA (5 Die)



3D SIP Developments and Trends
Flynn Carson
STATS ChiPAC
IMAPS, DPC, 2007
</td>
<td>Sometimes SIP products look like a reinvention of the hybrid microcircuit, but in other cases there are significantly different technologies. Take these examples of how wire bonding has been used, not just to package a single semiconductor, but to create a vertical stack of multiple ICs.</td>
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The need for thermal management

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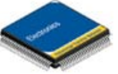
<td>Or this example, where a two-die stack has been combined with high-density additive-technology printed circuit construction to create a package that is very little bigger than the chip inside, which is the source of the CSP acronym meaning “Chip-Scale Package”.</td>
</tr>
<tr>
<td>
FLOMERICS
Industry Drivers & Trends
• System-in-Package (SiP): a new paradigm
– Embedded passives
– Multiple active & passive die
– Standard package outline
– Stacked Die, modules, MCMs
– Flexibility
– Faster time-to-market
– Lower non-recurring expenditure
– Higher performance

• New challenges arise from SiP
– Right first time substrate design essential
– Increased thermal density, EM interaction
Changing Role of CFD in Electronics Thermal Design
</td>
<td>As an idea, SIP is a lot more flexible, but it gives the challenges of getting the design right first time, and this is a more difficult challenge than building a product on a circuit board.

At the same time, one has to consider signal integrity issues and the possibility of greater unwanted interaction between circuit elements. And finally, from our perspective, there is also considerably increased thermal density when compared with the circuit board equivalent.</td>
</tr>
<tr>
<td>

So, how big is the problem?
▪ An increasing challenge!
▪ Total power increasing
▪ Dissipation density increasing
▪ Driven by applications
▪ Complicated by other changes
  ▪ board size
  ▪ layer count
  ▪ specialised package design
Electronics KTN – Knowledge For Growth
</td>
<td>So, how big is the problem? Well it’s clearly an increasing challenge, with total power increasing and dissipation density increasing. The thermal challenge is driven by applications, and made more complicated by changes at both board and component level.</td>
</tr>
</table>

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